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MSC-PoL: Hybrid GaN-Si Multistacked Switched Capacitor 48V PwrSiP VRM for Chiplets

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***Abstract*—This paper presents a multistack switched-capacitor point-of-load (MSC-PoL) voltage regulation module (VRM) with coupled magnetics for ultrahigh-current chiplet systems. In the MSC-PoL architecture, the stacked switched-capacitor cells split the high input voltage into several intermediate voltage rails, which are loaded with the switched-inductor cells to achieve soft charging and voltage regulation. Automatic capacitor voltage balancing and inductor current sharing are realized during the soft charging process. Many inductors of the switched-inductor cells are coupled into one and operated in interleaving to reduce the inductor current ripple and boost the transient speed. A 48-to-1-V/450-A VRM containing two MSC-PoL modules is built and tested, leveraging high voltage GaN devices for the front-end and high current Silicon devices for the back-end. Two ladder-structured coupled inductor designs are developed and compared, one of which installs a leakage magnetic plate to adjust the leakage inductance for lower current ripple. Featuring 3D stacked packaging, the entire power stage, gate drivers, and bootstrap circuits of one MSC-PoL module are enclosed into a $\frac{1}{16}$-brick/0.31-in^3/6-mm-thick package. The peak and the full-load efficiencies as well as the full-load power density (including both gate loss and size) of the MSC-PoL prototype with and without using the leakage plate are 91.7% and 89.5%, 85.8% and 85.6%, and 621 W/in^3 and 724 W/in^3, respectively. The 6-mm-thick MSC-PoL converter can be embedded into the chiplet or CPU socket, enabling power-supply-in-package (PwrSiP) for extreme efficiency, density, and control bandwidth.**

***Index Terms*—Switched capacitor, coupled inductor, point-of-load, CPU VRM, power-supply-in-package (PwrSiP), chiplet**

I. Introduction

As Dennard scaling tapered out, processor performance-per-watt improvement gained from the advances in fabrication process gradually faded away [1]–[3]. To meet the growing computational demand of artificial intelligent (AI) applications and cloud computing, microprocessors have entered a new era, where multiple cores are integrated on one chip and many chiplets are co-located on one interposer [4], incessantly pushing towards larger die area and higher power consumption. However, the continuous scaling of computing systems is hitting both the power wall and the memory wall (Fig. 1) [8]. With billions of transistors, high-performance microprocessors nowadays can consume hundreds of amperes of current at very low voltage (< 1 V), greatly increasing the conduction loss on power distribution networks (PDN) and narrowing the tolerance for supply voltage variations [9]. Besides, the development of AI algorithms dramatically boosts the memory bandwidth demand. Theses have brought severe challenges to designing highly sophisticated signal and power network, which requires high converter efficiency, high control bandwidth, and high signal and power integrity.

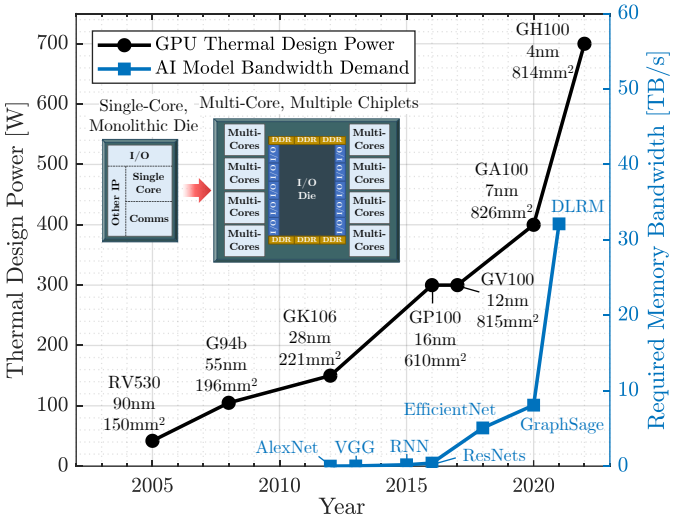

Fig. 1. As microprocessors develop from single-core, monolithic die to multi-core, multiple chiplets, modern computing systems are hitting both power wall and memory wall (replotted from [5]). Process node geometry and die area of selected high-performance-tier GPUs in [6], [7] are plotted along the scaling curve of GPU thermal design power.

A recent trend in data centers is to replace the ac power distribution with 48∼54 V dc distribution networks on the server racks [10]. To deliver power from 48 V dc bus to low voltage chiplets, conventional voltage regulation solutions heavily rely on the on-board power conversion with little or without any conversion stress inside the processor package (Fig. 2a). The on-board point-of-load (PoL) converters can be generally classified into two categories: the two-stage architecture [11]–[16] and the single-stage architecture [17]–[21]. In two-stage architectures, an intermediate dc voltage bus is employed to decouple the voltage conversion stress and transient dynamics between the two converter stages. The

This paper is an extension of a conference paper, "Multistack Switched-Capacitor Architecture with Coupled Magnetics for 48V-to-1V VRM," in *Proc. IEEE COMPEL*, 2022 [1]. (Corresponding Author: Minjie Chen.)

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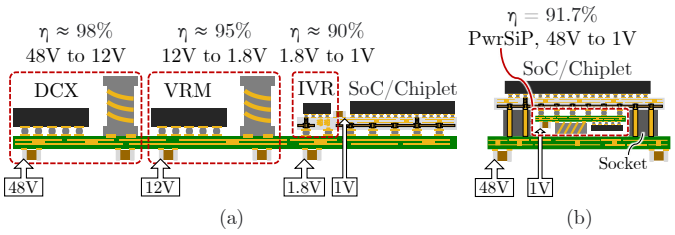

Fig. 2. Microprocessor power architecture comparison between (a) traditional solution that heavily relies on the on-board power conversion and (b) PwrSiP solution which features the in-package power conversion. A two-stage on-board conversion architecture is demonstrated in (a) as an example. Labeled efficiencies are sourced from [22]–[24] and this paper (including gate loss).

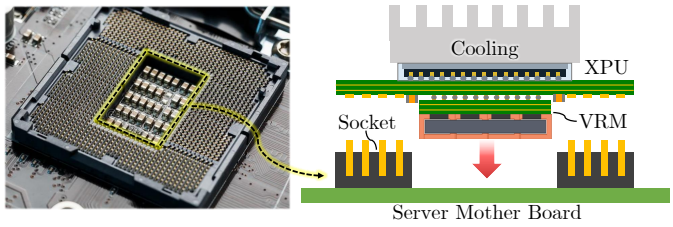

Fig. 3. Ultra-thin VRM embedded into a CPU package that fits in a land-grid array (LGA) socket for extreme efficiency, density, and control bandwidth.

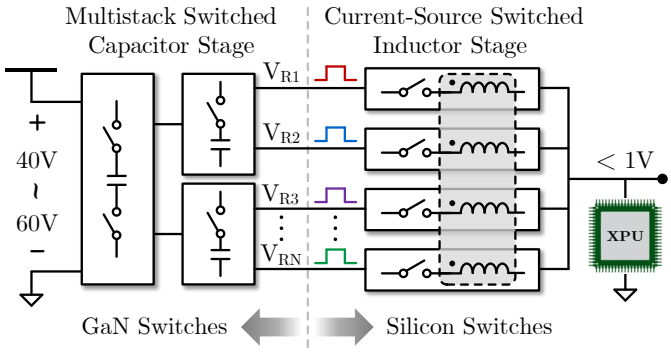

Fig. 4. MSC-PoL architecture for microprocessor voltage regulation. Stacked SC cells breakdown the high input voltage and create many intermediate voltage rails loaded with switched inductor cells to perform voltage regulation. Multiple capacitors of the SC stage are soft charged by one single coupled magnetic component. GaN switches can be utilized in the SC stage to undertake high voltage stress, while Silicon switches can be used in the regulation stage to undertake high current stress. The hybrid GaN-Si switch combination maximizes the advantages of the latest GaN FETs and Silicon MOSFETs [13], [30].

first stage is usually a transformer-based converter (e.g., LLC converter) or a switched-capacitor (SC) circuit functioned as a fixed-ratio dc transformer (DCX), and the second stage is a multiphase buck switching at high frequencies for the high control bandwidth. Compared to transformer-based topologies, SC converters utilize capacitors to undertake the major voltage stress for the large step-down ratio and can substantially reduce the converter size due to the superior capacitor energy storage density. By merging the two stages, one can soft charge the SC circuits to reduce the charge sharing loss [25]–[28], allowing the use of smaller capacitors or lower switching frequency. Single-stage architectures that have low component count and less power conversion stages can attain high efficiency and high power density, but they might experience difficulty realizing high control bandwidth. Although the on-board power conversion solutions are currently the mainstream due to mature techniques and easier implementation, their long PDN traces lead to high conduction loss and large on-board areas impede microprocessors from communicating with peripherals, limiting the efficiency, power density, as well as control and communication bandwidth.

An alternative 48-to-1-V voltage regulation solution is to embed a substantial part of or complete power conversion circuits into the processor package, enabling ultra-compact power-supply-in-package (PwrSiP) systems [29], as shown in Fig. 2b. With PwrSiP voltage regulation, power conversion stress is shifted from on-board circuits to in-package circuits. The shortened interconnection lengths can significantly reduce PDN losses and improve signal integrity, making it extremely attractive for powering future high-current microprocessors. Figure 3 shows an example PwrSiP implementation, where a voltage regulator module (VRM) is co-packaged with a chiplet or CPU. To fit into the chiplet/CPU socket, the VRM is required to have both small area and low z height. Typically, the VRM height is set by the magnetic components, whose sizes are limited by the fundamental trade-off between transient and ripple performance. Coupled magnetics with interleaving operation can obtain both high di/dt in transient and low current ripple in steady state, substantially reducing dc energy storage and magnetic size [31]–[34].

In pursuit of an ultra-compact chiplet/CPU VRM with miniaturized z height for PwrSiP power conversion, this paper presents a multistack switched-capacitor point-of-load (MSC-PoL) architecture with coupled magnetic components, as demonstrated in Fig. 4. Multiple SC cells are stacked in front and break down the high input voltage into many intermediate voltage rails, which are loaded with switched-inductor current sources to perform soft charging and voltage regulation. Different from the two-stage PoL architectures, the intermediate voltage rail herein is not necessarily a fixed dc bus but may step between several dc levels at different switching states [35], [36]. The dc rail voltage is provided by the capacitor network of the SC stage, and thus large intermediate bus capacitors can be eliminated. The switched-inductor cell is switched in at right time to get the desired voltage level. Many inductors of the switched-inductor cells are merged into one and operated in interleaving. Through soft charging multiple switched capacitors with one single coupled magnetic component, the MSC-PoL architecture can minimize both capacitor and magnetic size, achieving extremely low z-height as well as high efficiency and high transient speed.

To validate the MSC-PoL architecture, a 48-to-1-V, 6-mm-thick MSC-PoL VRM with 3D-stacked ladder-core coupled inductors is built and tested. A 0.8-mm-thick leakage magnetic plate is designed to adjust the leakage inductance for lower current ripple. The MSC-PoL VRM leverages a hybrid GaN-Si switch combination and encloses all components of power stage, bootstrap, and gate driver circuits into a $\frac{1}{16}$-brick module with 0.31 in^3 ultra-compact size. Two MSC-PoL modules can support up to 450 A load current with over 724 W/in^3 power density. The peak efficiency (including gate loss) of the MSC-

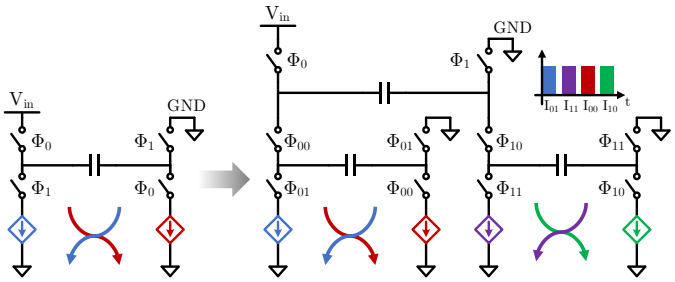

Fig. 5. MSC-PoL architecture based on modular H-bridge structures. Voltage conversion ratio can be extended by stacking more H-bridges. The switched-inductor current sources can be interleaved to reduce the output current ripple.

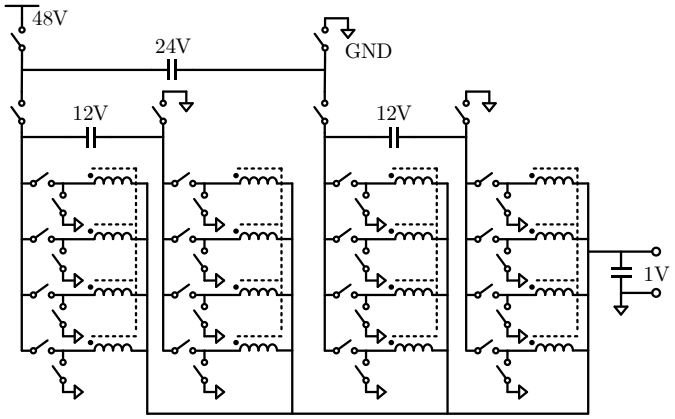

Fig. 6. An example implementation of the MSC-PoL architecture with the current sources implemented as parallel multiphase buck converters.

PoL prototype with and without using the leakage plate is 91.7% and 89.5% respectively.

The remainder of this paper is structured as follows. Section II introduces the multistack switched-capacitor architecture together with several example topology implementations. Section III presents a specific 48-to-1-V MSC-PoL topology, clarifies its working principles, and analyzes its dynamic performance with small-signal modelings. Section IV elaborates the design of the MSC-PoL converter, including the ladder-structured coupled inductor, gate driver circuits and 3D stacked packaging. Detailed experimental results are presented in Section V. Finally, Section VII concludes this paper.

II. Multistack Switched-Capacitor Architecture

There are many different ways of implementing the SC cells and the switched-inductor current sources of the multistack switched-capacitor architecture. The SC cells can be implemented as any SC structure that can leverage soft charging, such as Dickson derived topologies or flying capacitor derived topologies; the switched-inductor cells functioning as voltage regulators can be implemented as PWM or resonant converters, such as buck, series-capacitor buck (SCB), and SEPIC converters. One can combine different switched-capacitor and switched-inductor cells to meet diverse design requirements.

Figure 5 shows an MSC-PoL architecture based on modular "H-bridge" structures. The SC cell is configured as a 2:1 H-bridge circuit with one terminal connected to the input side, one terminal connected to ground, and two intermediate

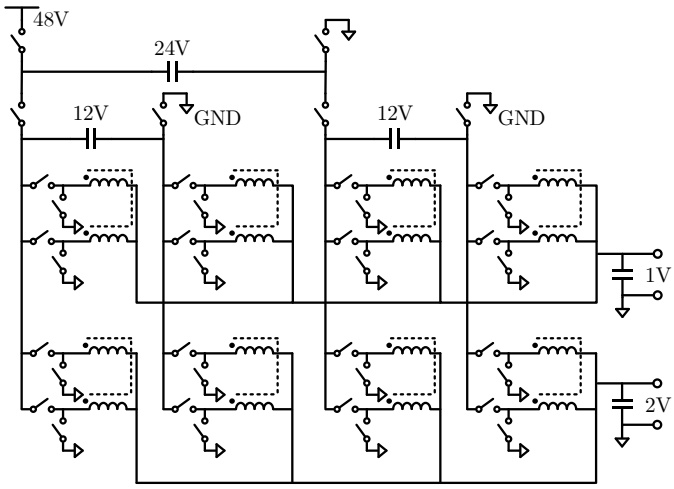

Fig. 7. An example implementation of the MSC-PoL architecture with multiple output ports for chiplets. The current sources can be separately regulated to supply different output voltage levels.

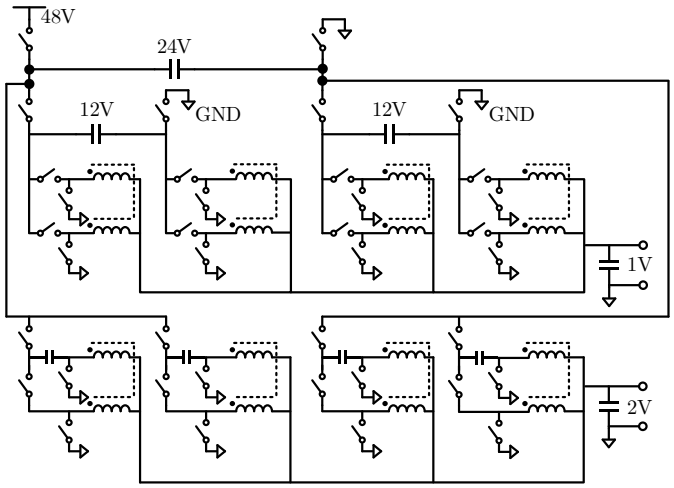

Fig. 8. An example implementation of the MSC-PoL architecture with multiple output ports for chiplets. The current sources can be tapped into different locations of the stacked SC circuits and can be implemented as different converters, such as multiphase buck and multiphase SCB.

voltage rails each providing a half of the input voltage. Two voltage rails are loaded with switched-inductor circuits that function as voltage regulators and can soft charge and discharge the flying capacitor of the H-bridge SC cell. The MSC-PoL architecture is modular and extendable. One can stack many H-bridge structures to interface with higher voltages (e.g., 96 V, 192 V), or parallel multiple voltage regulator structures to support higher output currents. Redundant switches within the stacked H-bridges or between the SC stage and the switched-inductor stage are merged to reduce component count and power loss [15]. The switched-inductor current sources are operated in interleaving to decrease the output current ripple.

Figures 6–8 show several example MSC-PoL topologies with sixteen output phases. The 16-phase inductors can be implemented as eight 2-phase coupled inductors, four 4-phase coupled inductors, or one 16-phase coupled inductor. The 16-phase switched inductor cells can be implemented as multiphase buck (Figs. 6 and 7), multiphase SCB, or a

hybrid (Fig. 8). Figure 7 shows an alternative implementation of the MSC-PoL architecture which is capable of producing multiple output voltages. The current sources are connected in parallel but are separately regulated to supply different output voltage levels. Figure 8 shows another example multi-output topology with current sources tapped into different locations of the stacked SC circuits. The switched-inductor current sources connected to higher levels of the SC circuits can provide higher output voltages. Benefiting from the stacked switched-capacitor/inductor structure, capacitor soft charging, coupled magnetics, and interleaving operation, the MSC-PoL architecture have following advantages:

- *Reduced Passive Component Size:* The MSC-PoL architecture enables transformerless voltage conversion with extremely higher power density because of: 1) reduced capacitor size owing to superior capacitor energy storage density and soft charging; 2) miniaturized magnetic component size by magnetics coupling; and 3) reduced filter size due to decreased output current ripple caused by interleaving. The greatly reduced passive component size makes the MSC-PoL architecture a very attractive solution to CPU/chiplet PwrSiP voltage regulation.
- *Improved Efficiency and Transient Speed:* Soft charging the flying capacitors reduces the capacitor charge sharing loss; coupled magnetics with interleaving operation decrease inductor current ripple, reducing both switching loss and conduction loss; the ultra-compact converter size enables PwrSiP voltage regulation with shortened interconnections, reducing the PDN conduction loss. Besides, the reduced coupled inductor current ripple allows the use of smaller leakage inductance with smaller inductive dc energy storage and faster transient speed.
- *Automatic Current Sharing and Voltage Balancing:* Mutual balancing between capacitor voltages and inductor currents can be achieved during the capacitor charging and discharging processes: 1) the flying capacitor voltage of the H-bridge SC cell and the two following switching cell currents are automatically balanced; 2) the blocking capacitor voltage of the switched-inductor cell (e.g., SCB and SEPIC) and parallel phase inductor currents are automatically balanced. Coupled magnetics can also suppress the unbalanced voltages and currents caused by nonideal factors including resistance variation between phases [37], phase shift error [38], and source impedance [39].

III. A 48-TO-1-V MSC-POL CPU VOLTAGE REGULATOR

This section presents the operation principles and small-signal models of a 48-V-to-1-V 450-A MSC-PoL converter.

A. Topology and Operation Principle

Figure 9 shows the 48-to-1-V MSC-PoL topology. It consists of one H-bridge SC cell stacking on top of two 4-phase SCB cells. The H-bridge SC cell steps down the V_{in} by half and distributes 24 V to each SCB cell. Two switches at the output terminals of the H-bridge are merged with the input switches of the SCB circuits. Voltage conversion ratios or

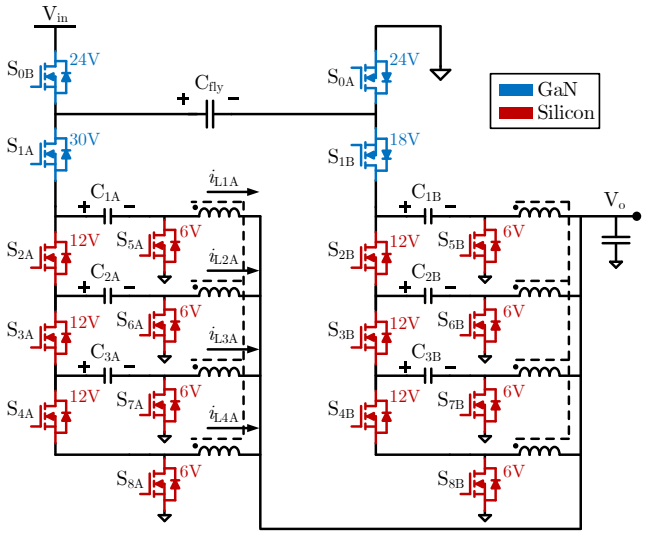

Fig. 9. Topology of the 48-to-1-V MSC-PoL converter. One 2:1 H-bridge SC cell is stacked in front and drives two 4-phase SCB cells. GaN FETs are plotted in blue and Silicon MOSFETs are plotted in red. Maximum voltage stress of each switch is labeled aside.

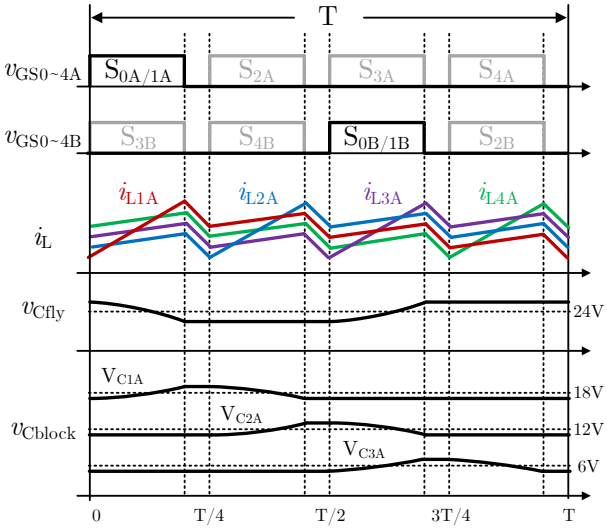

Fig. 10. Key steady-state operation waveforms of the 48-to-1-V MSC-PoL converter. Inductor currents and blocking capacitor voltages of the SCB cell A are plotted. Two SCB cells are interleaved by 180° phase shift as an example.

power ratings can be extended by stacking more H bridges or paralleling more series-capacitor buck phases [35]. In Fig. 9, the maximum drain-source voltage stress is labeled aside each switch. Switches in the H-bridge SC cell can use high voltage GaN FETs to undertake high voltage stress, while switches in the SCB cells can utilize low voltage, low resistance Silicon MOSFETs to support large current output.

Figure 10 plots key steady-state waveforms of the 48-to-1-V MSC-PoL converter. Switches S_{0A} & S_{0B} are synchronized with S_{1A} & S_{1B} respectively. High-side and low-side switches of each SCB phase are driven by complementary gate signals and four phases of each SCB cell are interleaved by 90° phase shifts. The four interleaving-operated inductors are coupled in parallel, leading to reduced inductor current ripples of 4x switching frequency. In Fig. 10, two SCB cells are operated

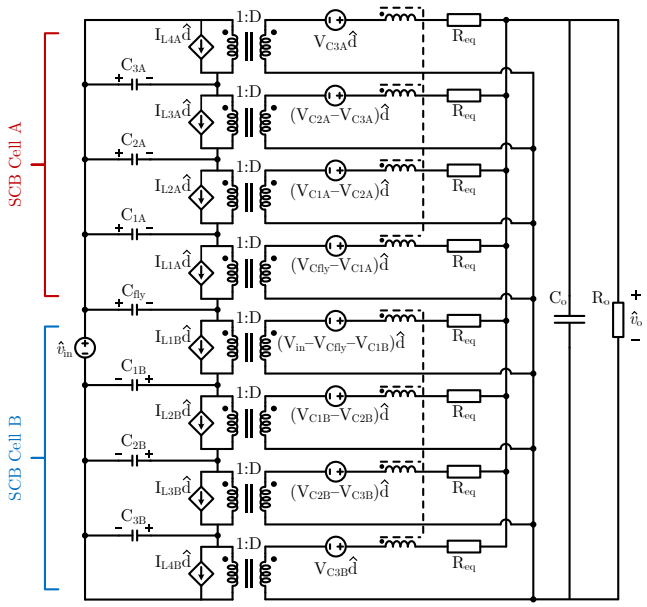

Fig. 11. Small-signal circuit model of the 48-to-1-V MSC-PoL converter.

with a 180° phase shift as an example. Other phase shifts between SCB cells (e.g., 145° or 225°) and alternative coupled inductor solutions (e.g., coupling all eight inductors in parallel) can also be applied to realize eight-phase interleaving with further reduced ripple amplitudes and increased ripple frequency for inductor and output currents. The flying capacitor C_{fly} in the H-bridge SC cell is soft charged and discharged in turns by the first two SCB phases (i.e., phases 1A and 1B), while the blocking capacitors $C_{1X\sim3X}$ in each SCB cell are soft charged and discharged by neighboring inductor currents. As a result, the 48-to-1-V MSC-PoL topology is capable of automatic voltage balancing for all the capacitors and automatic current sharing for all the parallel output branches.

Based on inductor volt-second balance, the steady-state output voltage can be expressed as:

$$V_o = \frac{D}{8} V_{in}. \tag{1}$$

$D = \frac{1}{6}$ for the 48:1 voltage conversion ratio. As indicated by Eq. (1), the steady-state operation of the MSC-PoL converter resembles that of a multiphase buck converter, but with a reduced input voltage of one eighth the original value.

B. Dynamic Modeling and Analysis

This subsection analyzes the transient performance of the MSC-PoL converter through small signal modeling. For the 4-phase coupled inductor, dynamic winding voltages and currents are associated by an inductance matrix:

$$\begin{bmatrix} v_{L1} \\ v_{L2} \\ v_{L3} \\ v_{L4} \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L_{34} \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{di_{L4}}{dt} \end{bmatrix}. \tag{2}$$

Two effective discrete inductances, the transient inductance (L_{tr}) and the steady-state inductance (L_{ss}), can be defined, which have the same transient speed and the same current ripple as the coupled inductor respectively [32]. If the 4-phase coupled inductor is symmetrically coupled, the summation of each column in the inductance matrix is the transient inductance for each phase: $L_{tr} = \sum_{j=1}^{4} L_{jk}$ $(k = 1 \sim 4)$.

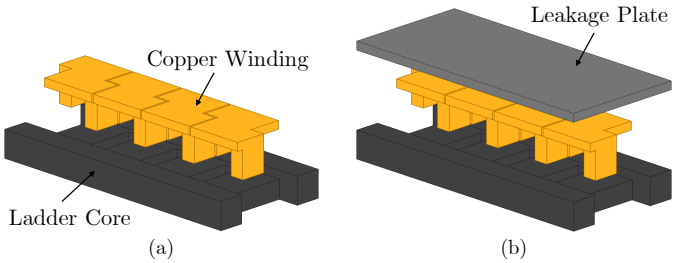

Fig. 12. Two four-phase coupled inductor designs based on (a) a ladder core and (b) a ladder core plus a leakage plate. The ladder core is made of DMR51W ($\mu_r = 900$), while the leakage plate is made of DMR53 ($\mu_r = 900$), a higher frequency magnetic material to enhance the leakage flux path.

Applying switching-cycle averaging and small-signal approximation to the MSC-PoL converter yields the small-signal circuit model as demonstrated in Fig. 11. It can be treated as the combination of two SCB small-signal circuits [40] linked by the flying capacitor C_{fly}. R_{eq} is the equivalent series resistance at each phase that captures the power losses. Based on Eq. (2) and Fig. 11, the overall converter dynamics can be modeled as:

$$D\cdot\hat{v}_{in} + V_{in}\cdot\hat{d} - (R_{eq} + sL_{tr}) \underbrace{\sum_{k=1}^{4} \left(\hat{i}_{LkA} + \hat{i}_{LkB}\right)}_{\hat{i}_o} = 8\hat{v}_o. \tag{3}$$

In Eq. (3), impacts of both the flying capacitor and the blocking capacitors are eliminated as summing up the dynamic equations for the eight phases. Detailed derivations are provided in Appendix I. Accordingly, the input-to-output and the control-to-output transfer functions are:

$$\begin{aligned} G_{v_{in}v_o} &= \frac{\hat{v}_o}{\hat{v}_{in}} = \frac{DR_o}{L_{tr}R_oC_o} \cdot \frac{1}{s^2 + 2\xi\omega_n s + \omega_n^2}, \\ G_{dv_o} &= \frac{\hat{v}_o}{\hat{d}} = \frac{V_{in}R_o}{L_{tr}R_oC_o} \cdot \frac{1}{s^2 + 2\xi\omega_n s + \omega_n^2}, \\ \omega_n &= \sqrt{\frac{R_{eq} + 8R_o}{L_{tr}R_oC_o}}, \quad \xi = \frac{L_{tr} + R_{eq}R_oC_o}{2\sqrt{L_{tr}R_oC_o(R_{eq} + 8R_o)}}. \end{aligned} \tag{4}$$

Eqs. (3) – (4) indicates that the overall system dynamics and transfer functions of the MSC-PoL converter are the same as a multiphase buck with $\frac{v_{in}}{8}$ input voltage and $\frac{L_{tr}}{8}$ output inductance. Therefore, it can be controlled by typical control methods for a multiphase buck (e.g., voltage mode control or constant-on-time control), expect that the duty ratio is limited within 25% which might restrain its maximum transient speed.

IV. Converter Design with 3D Stacked Packaging

To validate the MSC-PoL architecture, a 48-to-1-V, 450-A, 6-mm-thick MSC-PoL VRM with 3D-stacked ladder-core coupled inductors is built and tested. This section elaborates the design of the ultra-thin MSC-PoL VRM, including coupled inductors, gate driver circuits, and 3D stacked packaging.

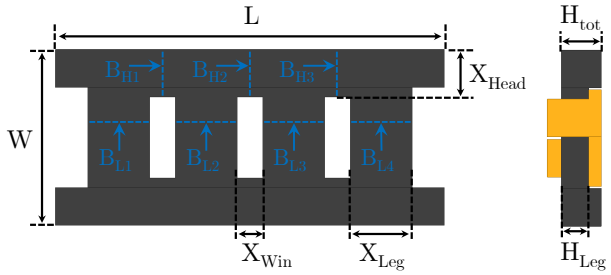

Fig. 13. Annotated design dimensions for the ladder core. To fit the PCB layout, the entire inductor shape can be determined by three dimension variables: X_{Leg}, H_{Leg}, and H_{tot}. Predicted core loss for geometry optimization is based on the flux density in each core segment (labeled in blue) using iGSE.

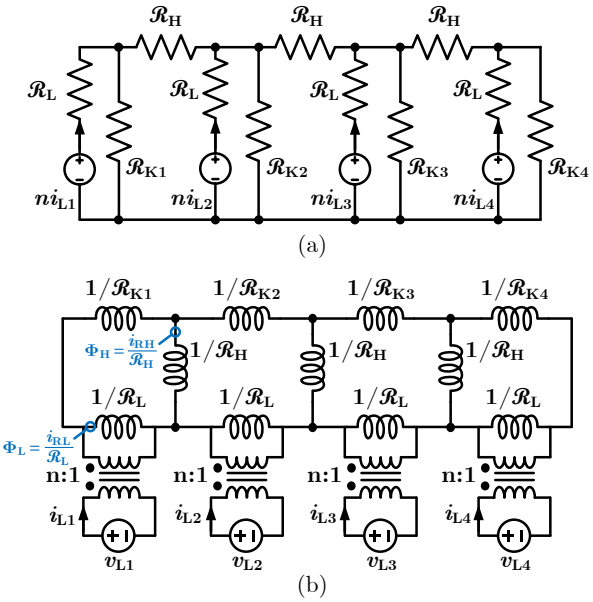

Fig. 14. Equivalent magnetic models for a ladder-structured coupled inductor: (a) magnetic circuit model; (b) inductance dual model. The magnetic flux in each core segment can be calculated through probing the current in the inductance dual model and dividing it by the corresponding reluctance. For the designed coupled inductors, the turns ratio $n = 1$.

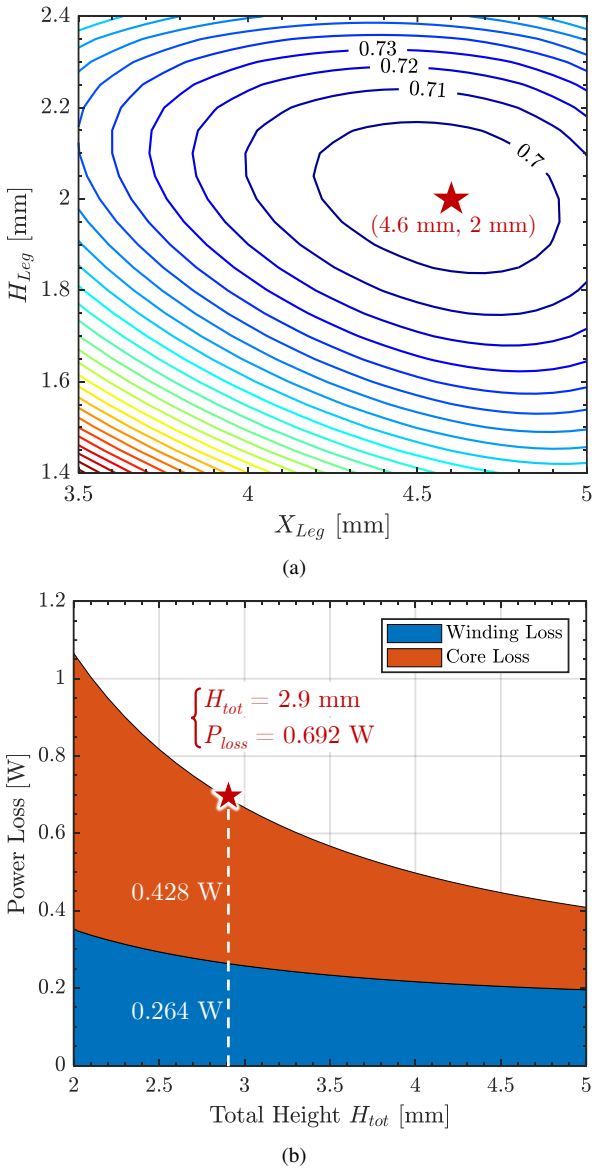

Fig. 15. Optimization process for the ladder-core coupled inductor: (a) total inductor loss contour plot at a specific H_{tot}; (b) optimized inductor loss versus H_{tot}. Core loss and conduction loss are optimized for one coupled inductor (four-phase) supporting 125 A at 500 kHz switching frequency.

A. Ladder-Structured Coupled Inductor

In the 48-to-1-V MSC-PoL converter, each SCB cell requires a four-phase coupled inductor. Figure 12 shows two ladder-structured coupled inductor designs based on: (1) a ladder core only; and (2) a ladder core plus a leakage plate. The ladder magnetic core, made of DMR51W ($\mu_r = 900$), couples four horizontally arranged windings in parallel. Stacking the leakage plate on top creates a low-reluctance path for the leakage magnetic flux, and the resulting larger leakage inductance can reduce the inductor current ripple, achieving higher efficiency. In a fully symmetric coupled inductor structure, the frequency of the leakage magnetic flux is four times the switching frequency. As a result, the leakage plate adopts a higher frequency magnetic material DMR53 ($\mu_r = 900$) for lower core loss.

Figure 13 annotates the design dimensions for the ladder core. Due to PCB layout constraints, the overall core and winding shapes are determined by three free dimension variables: X_{Leg}, H_{Leg}, and H_{tot}. In this paper, geometries of the ladder core are optimized for the minimum sum of conduction loss and core loss. Since the ac root-mean-squared (RMS) current is negligible at heavy load, the winding conduction loss is calculated only based on the dc resistance (DCR). The core loss is predicted using the improved Generalized Steinmetz Equations (iGSE) [41], where the power loss density of each core segment can be expressed as:

$$P_v = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt, \tag{5}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}. \tag{6}$$

k, α, and β are the material Steinmetz coefficients provided by the manufacturer. It is noticeable that the predicted core loss from iGSE does not capture the impacts of temperature and

TABLE I
PARAMETERS FOR THE OPTIMAL COUPLED INDUCTOR DESIGN

Parameter	Value
Total Length, L	28.9 mm
Total Width, W	13 mm
Total Height, H_{tot}	2.9 mm
Leg Width, X_{Leg}	4.6 mm
Leg Height, H_{Leg}	2 mm
Window Width, X_{Win}	1.9 mm
Header Width, X_{Head}	3.5 mm
Leg Reluctance, $\mathcal{R}_L$	0.91×10^6 H^{-1}
Header Reluctance, $\mathcal{R}_H$	1.21×10^6 H^{-1}
Leakage Reluctance, $\mathcal{R}_K$*	① $52.1 \sim 65.9 \times 10^6$ H^{-1} ② $12.5 \sim 14.1 \times 10^6$ H^{-1}

* Simulated leakage reluctance per phase: ① is for the design with ladder core only; ② is for using ladder core plus leakage plate.

TABLE II
COMPARISON BETWEEN THE TWO FOUR-PHASE COUPLED INDUCTORS

Inductor Design	Height	L_{tr}*	L_{ss}*	DCR†	Current Rating
Ladder Core	2.9 mm	17 nH	140 nH	0.06 mΩ	$>$ 125 A
Ladder Core + Leakage Plate	3.9 mm	75 nH	381 nH	0.06 mΩ	$>$ 125 A

* L_{tr} and L_{ss} are simulated average values for each phase when D = 1/6.
† DCR is measured winding dc resistance per phase.

dc flux density, and the calculated winding conduction loss does not include the loss from winding soldering and winding returning path on the PCB board. However, the resistance of soldering and PCB returning path is less dependent on inductor geometry and is relatively constant. Therefore, the calculated inductor loss herein can still provide good guidance for optimizing the dimensions of the coupled inductor. Advanced core loss modeling tools, such as neural network models, can be used to estimate the core loss under particular operating conditions (e.g., waveform, temperature, dc-bias) [42].

In Eq. (5), the flux density of each core segment can be calculated based on the equivalent magnetic models in Fig. 14. Figure 14a plots the magnetic circuit model. Each core leg is modeled as a leg reluctance $\mathcal{R}_L$ in series with an MMF source. The top and bottom core segments between two legs are lumped as a header reluctance $\mathcal{R}_H$. The leakage flux path of each phase is modeled as a parallel leakage reluctance $\mathcal{R}_K$. Generally for a ladder-structured coupled inductor, $\mathcal{R}_K$ is not identical for all the phases. The $\mathcal{R}_K$ discrepancy tends to increase as phase number increases, but for the designed four-phase coupled inductor, the difference is small enough and $\mathcal{R}_K$ can be analyzed using average values in most of the cases. Adding the leakage plate will reduce $\mathcal{R}_K$, but it is still much larger than the core reluctance $\mathcal{R}_L$ and $\mathcal{R}_H$. Applying circuit duality to the magnetic circuit model yields the inductance dual model as shown in Fig. 14b. Magnetic flux in each core segment can be calculated through probing the current in the inductance dual model and dividing it by corresponding reluctance. Detailed derivations of the magnetic flux density are provided in Appendix II.

Figure 15 demonstrates the optimization process for the

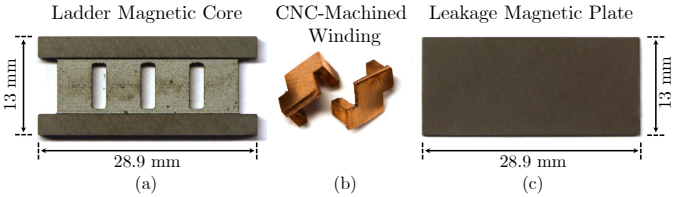

Fig. 16. Customized magnetic components: (a) four-phase ladder magnetic core (DMR51W, $\mu_r = 900$); (b) CNC-machined windings; (c) leakage magnetic plate (DMR53, $\mu_r = 900$).

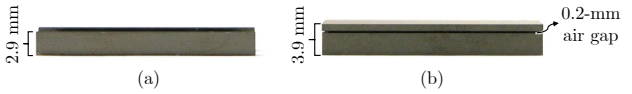

Fig. 17. Coupled inductor height of: (a) using the ladder core only; (b) using the ladder core plus the 0.8-mm leakage plate with a 0.2-mm air gap.

ladder-core coupled inductor (without the leakage plate) under the conditions of 125 A average current (31.25-A/phase) and 500 kHz switching frequency. Given a specific inductor height H_{tot}, the optimized inductor geometries are obtained from the inductor loss contour plot by sweeping X_{leg} and H_{leg} as shown in Fig. 15a. The optimized inductor loss versus H_{tot} is plotted in Fig. 15b. Weighing the tradeoff between inductor loss and height, H_{tot} is selected as 2.9 mm. Key parameters for the optimal coupled inductor design are listed in Table I. Figures 16 and 17 shows the CNC-machined magnetic cores and copper windings based on the optimized geometries. The ladder core measures 28.9 mm $\times$ 13 mm $\times$ 2.9 mm. A customized 0.8-mm magnetic plate can be put on top of the ladder core with 0.2-mm air gap for enhanced leakage flux. Comparison of the two coupled inductors is summarized in Table II. Notice that the transient inductance is equivalent to the leakage inductance for the two parallel coupled inductors.

The two coupled inductor structures are verified by both FEM and SPICE simulations. Figure 18 shows the FEM magnetic field simulation in ANSYS. In Fig. 18a, a magnetostatic simulation is performed to display the dc flux distribution when each phase conducts 31.25 A dc current (125 A in total). The dc flux density in the core leg is 0.066 T if not using the leakage plate. After installing the leakage plate, it increases to 0.28 T, but it is still much lower than the saturation flux density (0.5 T) of the magnetic material used. Therefore, both the two coupled inductors can support 125 A dc current, which is sufficient for the MSC-PoL converter designed in this paper. Although adding the leakage plate will reduce the saturation current limit, it is acceptable in most cases because the current rating of a coupled inductor is usually constrained by unbalanced phase currents and semiconductor devices. In Fig. 18b, a transient magnetic field simulation is conducted for one switching cycle (2 μs), displaying the ac flux density at $t = 1$ μs when it reaches its peak in the middle core header and the third core leg. Detailed simulated ac flux density versus time is provided in Appendix II. As shown in Fig. 18b, the ac flux density is similar with or without using the leakage plate. This indicates the core losses of the two coupled inductors are comparable, though they might be influenced by the dc bias.

Figure 19 shows the SPICE simulation of the 48-to-1-V

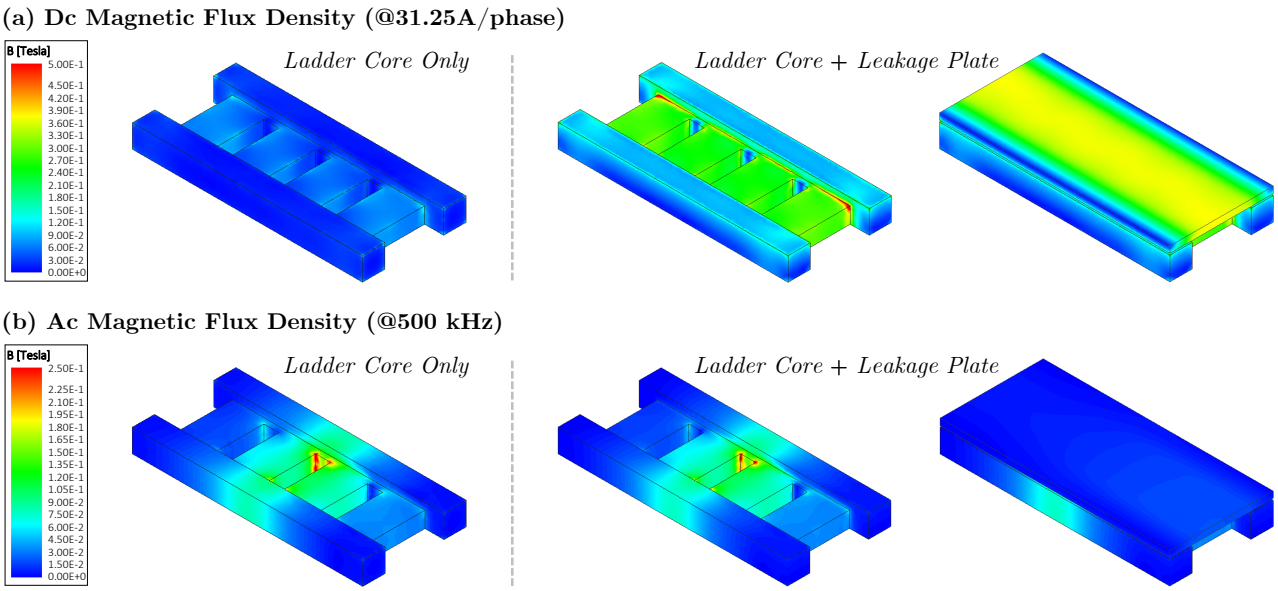

Fig. 18. ANSYS FEM simulation of the two coupled inductor designs: (a) dc flux density distribution when supporting 31.25 A average current per phase (125 A in total) and (b) ac flux density distribution at the middle of one switching cycle. $V_{in} = 48$ V, $V_o = 1$ V, $f_{sw} = 500$ kHz.

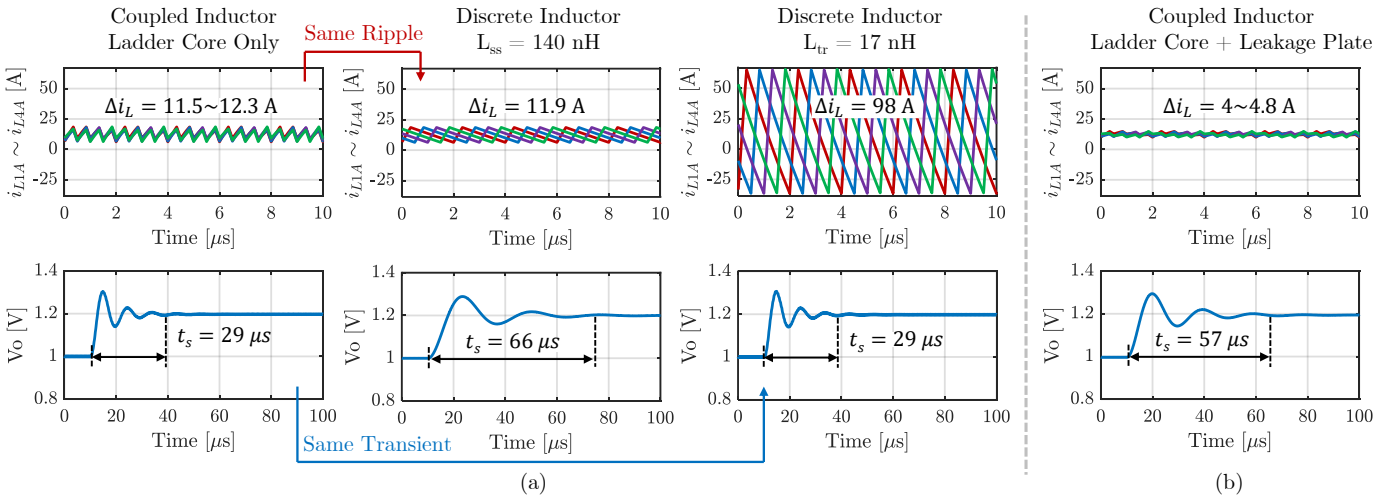

Fig. 19. Simulated steady-state inductor currents and transient output voltages during a duty ratio step change when using: (a) the coupled inductor with ladder core only and discrete inductors of its equivalent L_{ss} and L_{tr}; (b) the coupled inductor with ladder core plus leakage plate. $V_{in} = 48$ V, $V_o = 1 \rightarrow 1.2$ V, $f_{sw} = 500$ kHz, $R_{eq} = 3$ mΩ, $R_o = 0.01$ Ω, $C_o = 1$ mF. (Steady-state inductor currents are simulated at $V_o = 1$ V).

MSC-PoL converter when using different coupled inductor designs as well as discrete inductors of equivalent L_{ss} and L_{tr}. Simulations with coupled inductors are based on the extracted inductance matrix from ANSYS. Simulated steady-state inductor current ripples and transient output voltages during a duty ratio step change are plotted in the figure. Since the transfer function G_{dv_o} in Eq. (4) is a second-order system, its maximum percent overshoot (M_p) and 2% settling time (t_s) of a step response are:

$$M_p = e^{\frac{-\pi\xi}{\sqrt{1-\xi^2}}}, \quad t_s = \frac{4}{\xi\omega_n} = \frac{8R_oC_o}{1+\frac{R_{eq}R_oC_o}{L_{tr}}}. \tag{7}$$

Lower L_{tr} results in faster transient with less t_s, but M_p is not necessarily smaller, for it is also related to other circuit parameters. Therefore, as implied by Fig. 19a, the ladder-core coupled inductor can achieve as fast transient speed as using small 17-nH discrete inductors while maintaining as low current ripple as using large 140-nH discrete inductors. If adding the leakage plate with 1-mm extra thickness, the coupled inductor can further reduce current ripple to an extremely low level (Fig. 19b), significantly decreasing switching related loss and improving converter efficiency. The disadvantages of adding the leakage plate are slower transient speed, lower saturation current limit, and larger thickness.

B. Gate Driver Circuits and 3D Stacked Packaging

Table III tabulates key component parameters of the 48-to-1-V MSC-PoL module. GaN switches with higher voltage ratings are used for $S_{0X} \sim S_{1X}$ in the SC cell to undertake high voltage stress; Silicon MOSFETs with lower voltage

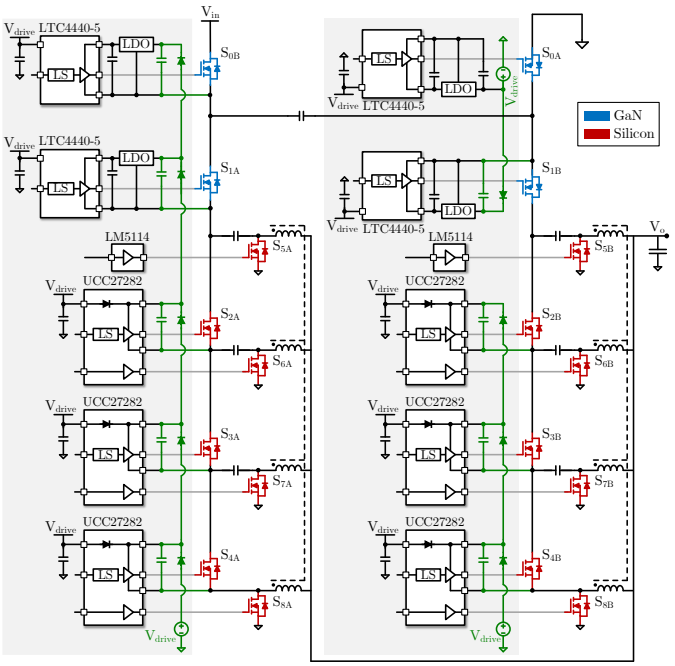

Fig. 20. Design of gate driver circuits and bootstrap chains (plotted in green) for one MSC-PoL module. All gate driver and bootstrap circuits are laid out together with the power stage inside the compact converter package.

TABLE III
BILL-OF-MATERIAL OF THE 48-TO-1-V MSC-POL CONVERTER

Semiconductor Devices	Description
Switches, $S_{0X} \sim S_{1X}$	EPC 2065
Gate Drivers for $S_{0X} \sim S_{1X}$	ADI LTC4440-5
LDO Regulators	On-Semi NCP711
High-Side Switches, $S_{2X} \sim S_{4X}$	Infineon BSZ0902NS
Low-Side Switches, $S_{5X} \sim S_{8X}$	Infineon BSZ011NE2LS5I
Gate Drivers for S_{5X}	TI LM5114
Gate Drivers for $S_{2X/6X} \sim S_{4X/8X}$	TI UCC27282

Capacitors*	Description
C_{in}	0805 X5R 100 V 4.7 μF × 36, C_{eff} = 20.3 μF
C_{fly}	0805 X5R 35 V 22 μF × 22, C_{eff} = 38.7 μF
C_{1X}	0805 X5R 25 V 22 μF × 9, C_{eff} = 20 μF
C_{2X}	0805 X5R 25 V 22 μF × 7, C_{eff} = 27.7 μF
C_{3X}	0805 X5R 25 V 22 μF × 6, C_{eff} = 52 μF
C_o	0805 X5R 6.3 V 100 μF × 12, C_{eff} = 0.94 mF

* Capacitor count and C_{eff} are listed for one MSC-PoL module.

ratings are used for $S_{2X} \sim S_{8X}$ in the SCB cells to undertake high current stress. The hybrid GaN-Si switch combination maximizes the advantages of material characteristics and state-of-the-art performance of GaN FETs and Silicon MOSFETs.

Figure 20 plots the detailed gate driver and bootstrap circuit design for one MSC-PoL module. Supporting by an external voltage rail V_{drive} ($V_{drive} = 8$ V), the bootstrap chain creates multiple floating dc voltages referenced to floating switch source terminals. In each SCB cell, half-bridge gate drivers (UCC27282) are used to drive $S_{2X} \sim S_{4X}$ and $S_{5X} \sim S_{8X}$, and low-side gate drivers (LM5114) are used to drive S_{5X}. In the H-bridge SC cell, high-side gate drivers (LTC4440-5) and 5-V LDOs are utilized for driving the GaN switches

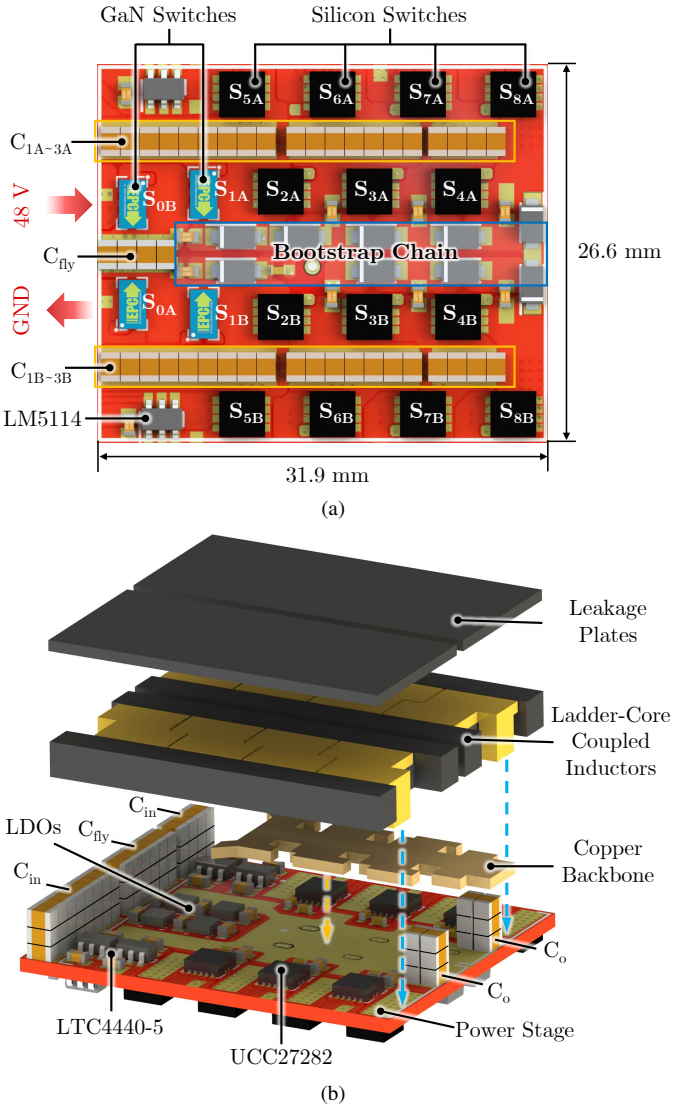

Fig. 21. PCB layout and 3D stacked packaging of the MSC-PoL VRM: (a) annotated top view; (b) annotated bottom assembly view. The PCB area is 31.9 mm × 26.6 mm = 848.54 mm^2, and the total VRM height is only 6 mm (7 mm if including the leakage plate).

$S_{0X} \sim S_{1X}$. The PWM input side of each gate driver is ground referenced and powered by V_{drive}. The driving output side is powered by the bootstrap chain for the floating switches or by V_{drive} for the grounded switches.

Detailed PCB layout and 3D stacked packaging of the MSC-PoL VRM are plotted in Fig. 21. The VRM measures 31.9 mm × 26.6 mm in area, and the overall height is only 6 mm (7 mm if including the leakage plate). All power devices are placed on the top side of the PCB, while the coupled inductors and gate drivers are stacked on the bottom side. Placing all power components on one side simplifies the cooling requirements by enabling single-sided heat dissipation. The bootstrap circuit chain is laid out in the center of the converter, and on its two sides symmetrically locates the H-bridge SC cell as well as the two 4-phase SCB cells (cells A&B). To minimize both converter height and on-board area, a 3D stacked inductor-driver packaging is implemented as

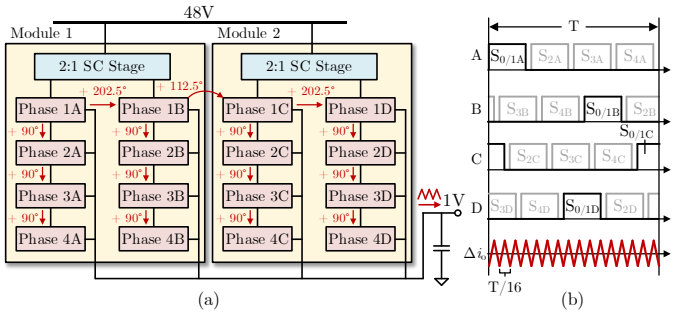

Fig. 22. (a) Block diagram of the prototype power stage. (b) An example phase shift strategy, which enables 16-phase interleaving with multiplicated ripple frequency ($16 \times f_{sw}$) and reduced ripple amplitude of the output current. Other phase shift schemes may also apply.

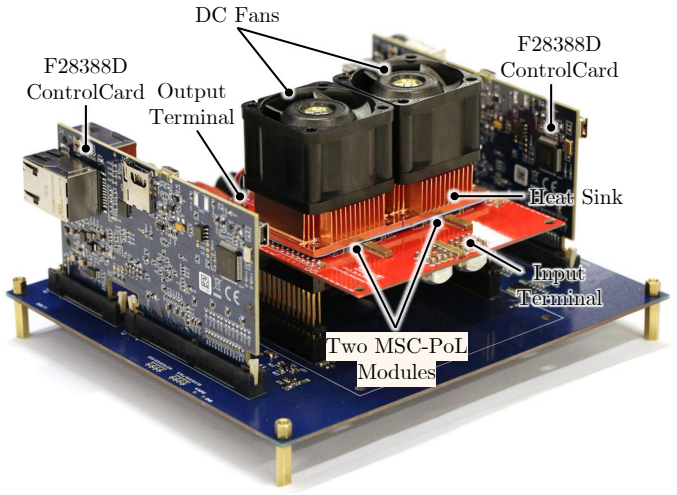

Fig. 23. Picture of the 48-to-1-V/450-A MSC-PoL prototype containing two MSC-PoL modules, a signal interface board, and two microcontroller boards. Each MSC-PoL module is covered by a heat sink together with a DC fan, which can easily dissipate most of the heat of power components.

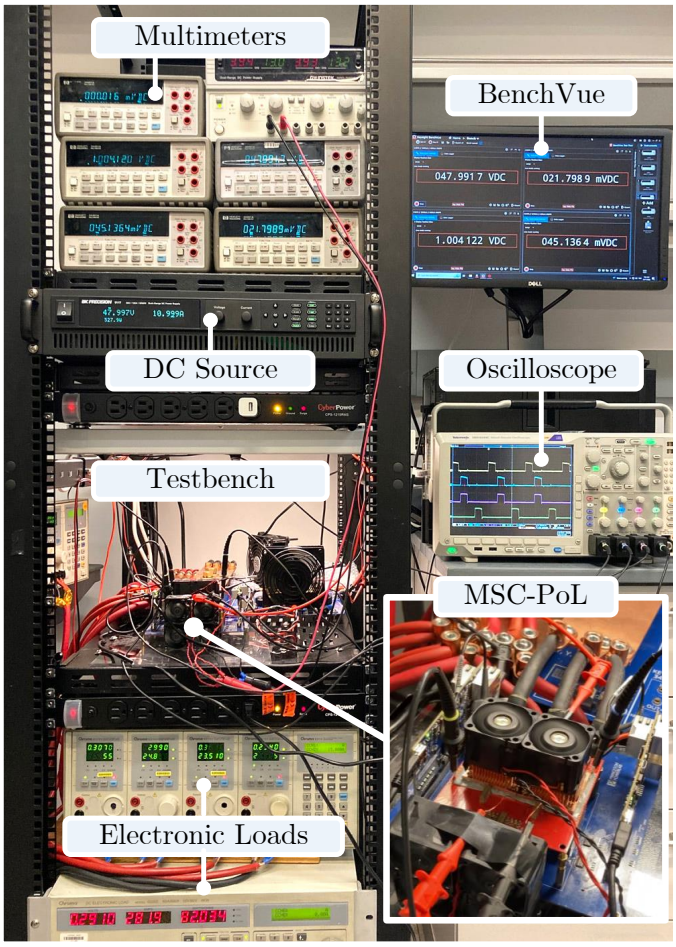

Fig. 24. Picture of the experimental testbench. Digital multimeters are interfaced with the BenchVue platform to automatically collect efficiency measurement results. Two current shunts are utilized for measuring the input and the output currents. A dc power source is used as the 48 V dc bus. Multiple electronic loads are connected in parallel to drain high load currents.

shown in Fig. 21b. At the bottom side of the PCB, the coupled inductors are stacked on top of the gate drivers with a copper backbone inserted in between to draw the high output currents out. Winding structures of the two inductors are in symmetry to bring all the output currents to the middle, which helps to shorten the layout length of PCB traces and reduce the conduction loss of the overall system. All components including power stage, bootstrap chain, gate driver circuits, and coupled inductors are packaged into a $\frac{1}{16}$-brick module with 0.31 in^3 ultra-compact size and 6-mm ulta-thin thickness. Only PWM pins, a voltage rail V_{drive}, and an optional heat sink are needed to operate the MSC-PoL VRM.

V. Experimental Results

A. Prototype and Testbench

A 48-to-1-V/450-A MSC-PoL prototype comprising two parallel-connected MSC-PoL modules are fabricated and tested. Figure 22a plots the block diagram of the prototype power stage, which contains 16 output phases. Appropriate phase shift strategy can be designed to achieve 16-phase interleaving with multiplicated ripple frequency and reduced ripple amplitude of the output current, as shown in Fig. 22b. Figure 23 shows the complete hardware prototype including the power stage, the signal interface board and two F28388D controllers. A heat sink (SKV38538514-CU) equipped with a DC fan (9GA0312P3J001) is placed on top of each MSC-PoL module through thermal interface. The heat sink covers all power devices placed on the top side of the PCB. Benefiting from the single-side heat dissipation, the heat sink can easily take away most of the heat generated by the power devices.

Figure 24 shows the experimental testbench. Four digital multimeters (Agilent 34401A) are utilized in combination with the BenchVue software platform to setup an automatic efficiency measurement system. Two current shunts (Rideon RSN-50 and RSC-1000), calibrated by Agilent 34330A, are connected in series at the input and output for precise current measurement. A dc power source (BK Precision 9117) is used to provide the 48 V input dc voltage. Multiple electronic loads (Chroma 63103A and 63203) are parallelly connected to drain high load currents from the converter.

Figure 25 exhibits the ultra-thin MSC-PoL VRM and its 3D stacked packaging process. As shown in Fig. 25a, each MSC-PoL module is enclosed within a 31.9 mm×26.6 mm×6 mm

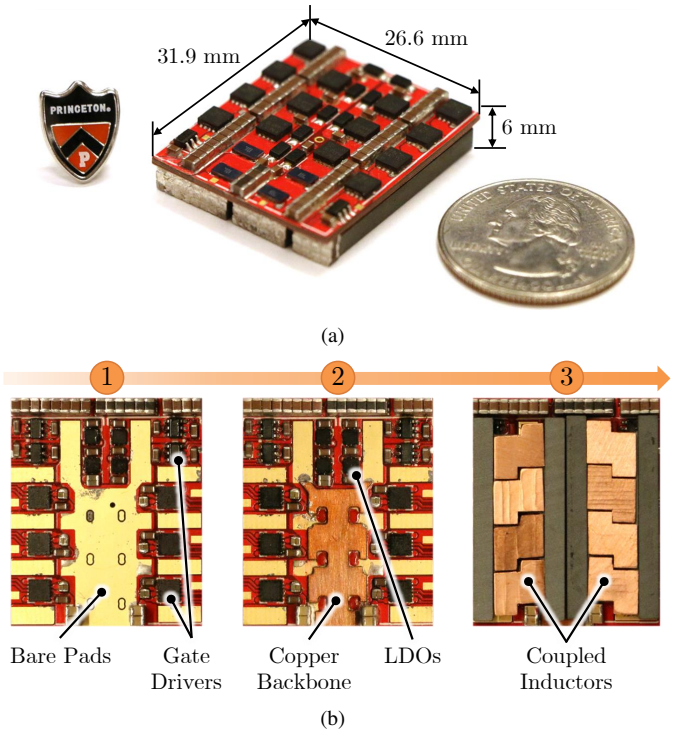

Fig. 25. (a) One MSC-PoL module (w/o leakage plate) compared with a U.S. quarter. (b) Packaging procedures of the 3D stacked inductor-driver structure.

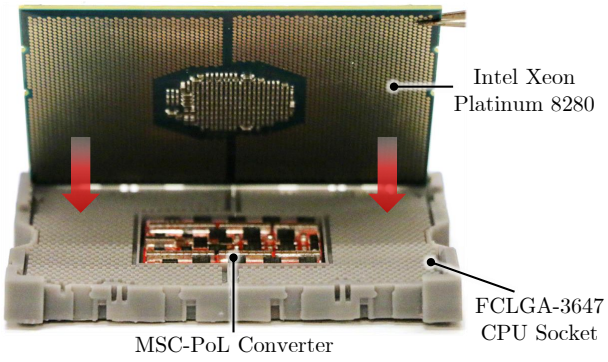

Fig. 26. Mechanical demonstration of a 225 W 48-to-1-V MSC-PoL module embedded into a 3D-printed FCLGA-3647 socket to support a server CPU (Intel Xeon Platinum 8280, 205 W).

box volume, which is comparable to a U.S. quarter. The step-by-step packaging procedures of the stacked inductor-driver structure is plotted in Fig. 25b. With the ultra-compact size and the ultra-thin thickness, the MSC-PoL VRM can be embedded into a FCLGA-3647 socket to power an Intel Xeon Platinum 8280 CPU (205 W), enabling PwrSiP voltage regulation as demonstrated in Fig. 26.

In the following experiments, the MSC-PoL prototype is tested based on the component parameters in Table III and phase shift strategy in Fig. 22b, unless otherwise specified. Measured experimental results when using different coupled inductor designs in Table II are compared and discussed.

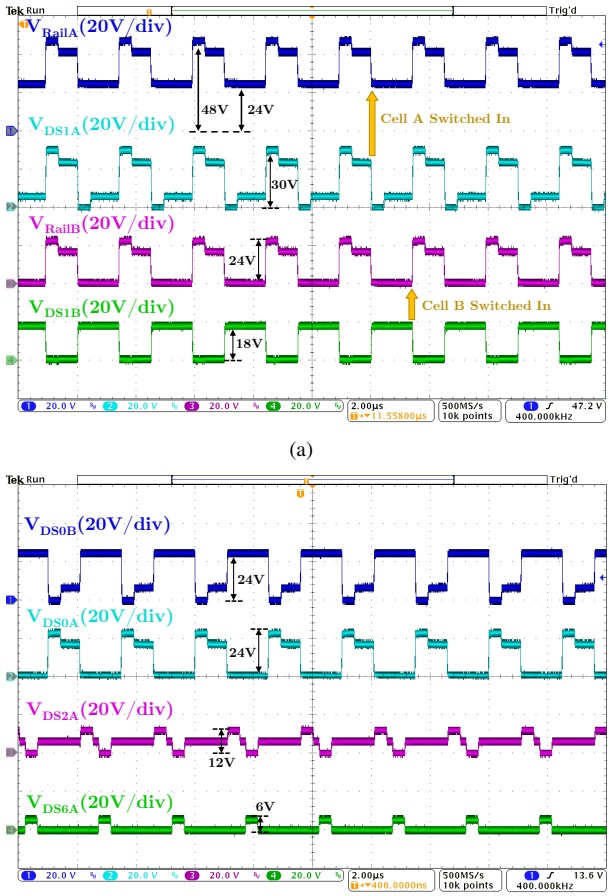

Fig. 27. Steady-state waveforms of switch drain-source voltages and intermediate rail voltages. V_{Rail1A} and V_{Rail1B} are the positive and the negative terminal voltages of the flying capacitor C_{fly}. $f_{sw} = 400$ kHz; $V_o = 1$ V.

B. Steady-State Operation

This subsection demonstrates the steady-state operation of the MSC-PoL prototype when delivering power from 48 V to 1 V and switching at 400 kHz. The leakage plate is installed on the coupled inductor for lower current ripple.

Figure 27 shows the measured waveforms of switch drain-source voltages and two intermediate rail voltages. The maximum switch voltage stresses are labeled aside the waveforms, which are 24 V for S_{0X}, 30 V for $S_{1A/C}$, 18 V for $S_{1B/D}$, 12 V for SCB high side switches ($S_{2X} \sim S_{4X}$), and 6 V for SCB low side switches ($S_{5X} \sim S_{8X}$), consistent with the analysis in Fig. 9. Two intermediate rail voltages V_{Rail1A} and V_{Rail1B} refer to the voltages of positive and negative terminals of the flying capacitor C_{fly}. V_{Rail1A} is shifting between 24 V and 48 V, while V_{Rail1B} is alternating between 0 V and 24 V. By turning on S_{1X}, each SCB cell will be switched into the corresponding voltage rail when it turns 24 V.

Figure 28 shows the measured waveforms of switch node voltages and output voltage ripples. The phase shift strategy in Fig. 22 is applied: (1) the phase shifts among four SCB cells are 202.5° between cells A&B, 112.5° between cells B&C, and 202.5° between cells C&D; (2) neighboring phases within each SCB cell are shifted by 90°. As shown in Fig. 28b,

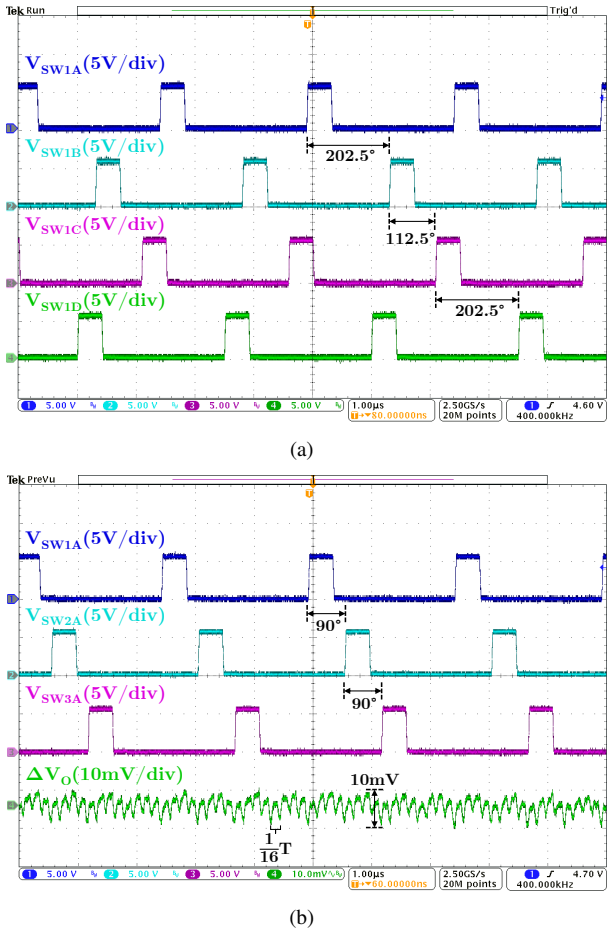

Fig. 28. Steady-state waveforms of switch node voltages and output voltage ripples. The 16-phase interleaving operation in Fig. 22 is applied, yielding $16f_{sw}$ ripple frequency for the output voltage. $f_{sw} = 400$ kHz; $V_o = 1$ V.

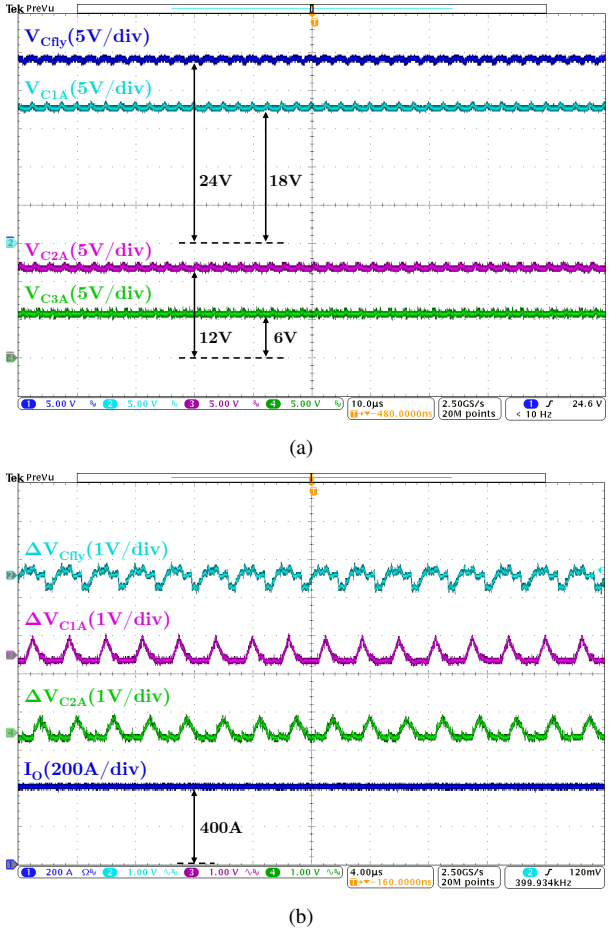

Fig. 29. Steady-state waveforms of: (a) capacitor dc voltages; (b) capacitor ac voltage ripples and output current. $f_{sw} = 400$ kHz; $V_o = 1$ V; $I_o = 400$ A.

the applied phase shift scheme enables 16-phase interleaving, yielding greatly reduced ripple amplitude with $16f_{sw}$ ripple frequency for the output voltage. The peak-peak steady-state output voltage ripple is less than 10 mV.

Figure 29 shows the measured capacitor dc voltages and ac voltage ripples when delivering 400 A load current. As indicated by Fig. 29a, both the flying capacitor and the blocking capacitors can maintain stable voltages at heavy load, functioning like a dc source with expected dc values. As shown in Fig. 29b, the capacitor ac voltage ripples can remain less than 0.8 V at 400 A load current (i.e., 89% of the full load).

C. Transient Performance

This subsection exhibits the open-loop and the closed-loop transient experiments tested on one MSC-PoL module with and without using the leakage plate. The transient experiments are performed when $V_{in} = 48$ V, $f_{sw} = 704$ kHz, $C_o = 3$ mF.

Figure 30 shows the measured transient waveforms during an open-loop duty ratio step change at 100 A load current. The duty ratio steps from 15.8% to 22.2%, yielding a step change V_o from 0.8 V to 1.2 V. The settling time of reaching within 5% error band of the final voltage is 26 μs for using the leakage plate and 18 μs for not using the leakage plate. As discussed in Section IV-A, adding the leakage plate will reduce the current ripple but also slow down the transient speed due to larger leakage inductance, resulting in longer settling time. However, one MSC-PoL module contains eight output phases in parallel. This narrows the transient performance difference between the two coupled inductor designs since both of them have a very small total output leakage inductance, which is comparable to the parasitic trace inductance. Therefore, after adding the leakage plate, the MSC-PoL VRM still maintains a fast transient speed. Besides, the flying capacitor and the blocking capacitor voltages remain stable during the open loop duty ratio step change.

Figure 31 shows the measured waveforms of closed-loop transient experiments. A typical voltage-mode feedback control with PI compensator is implemented, which changes the duty ratio based on the error between reference and output voltages. The output load current is programmed to step between 50 A and 150 A with 4 A/μs downslope. As indicated by the figure, the maximum voltage overshoot is less than 80 mV during this 100 A load step (44% of the full load). The flying capacitor and blocking capacitor voltages also remain stable in the closed-loop transient test. The transient performance can be further enhanced by increasing the control loop bandwidth (e.g., reducing the delay of controller

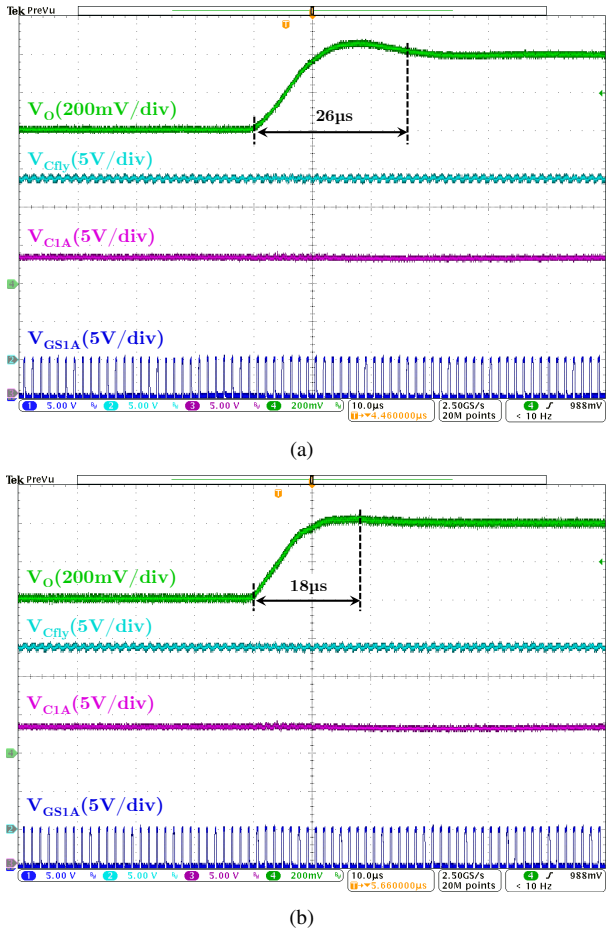

Fig. 30. Measured open-loop transient waveforms with one MSC-PoL module when (a) using the leakage plate and (b) not using the leakage plate. Duty ratio steps from 15.8% to 22.2%, yielding a step change V_o from 0.8 V to 1.2 V. $f_{sw} = 704$ kHz; $I_o = 100$ A; $C_o = 3$ mF.

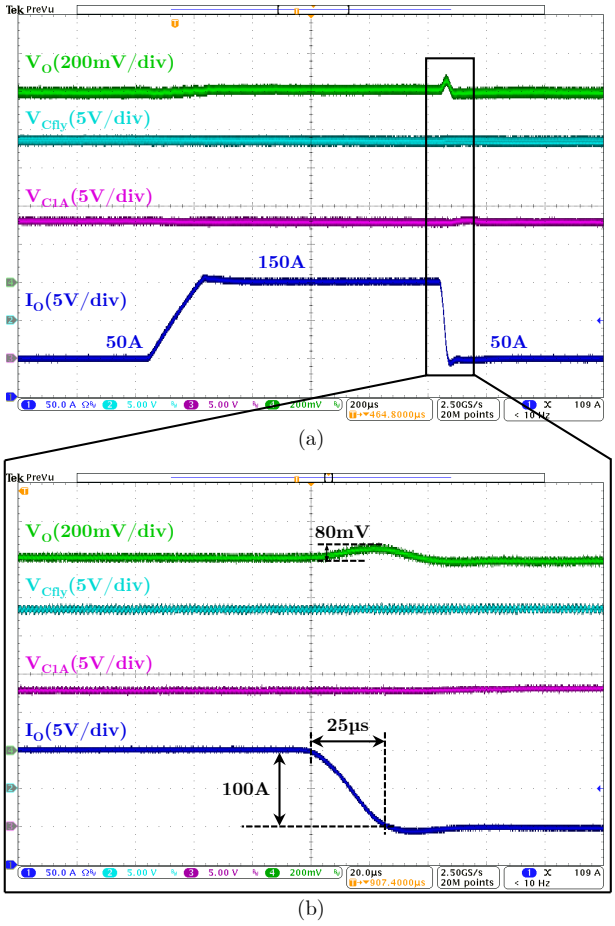

Fig. 31. Measured closed-loop transient waveforms with one MSC-PoL module (w/o the leakage plate) during a load step change between 50 A and 150 A. A typical voltage-mode feedback control is applied. The maximum voltage overshoot is less than 80 mV during the 100 A load step (44% of the full load) with 4 A/μs current slope. $f_{sw} = 704$ kHz; $C_o = 3$ mF.

and gate drivers) or by using advanced nonlinear controls (e.g., constant-on-time control). However, demonstrating the extreme transient performance of the converter is beyond the scope of this paper.

D. Efficiency Measurement

The efficiencies of the MSC-PoL prototype with and without using the leakage plate are measured at multiple switching frequencies. The gate drivers and the bootstrap chain are powered by an auxiliary dc-dc converter, and the gate losses are estimated by $Q_g V_{drive} f_{sw}$. V_{drive} is the voltage of the auxiliary power rail, and $V_{drive} = 8$ V in all experiments.

Figures 32 and 33 summarize the 48-to-1-V efficiencies of the MSC-PoL prototype with and without using the leakage plate respectively. Efficiencies of different switching frequencies excluding and including the gate losses are collected and compared. As shown in the figures, the MSC-PoL prototype with the leakage plate has a higher efficiency than without using the leakage plate. As the switching frequency increases, there is a tradeoff between the decreased ac conduction losses and the increased switching related losses (including switching losses, deadtime losses, parasitic loop inductance losses, etc.). When using the coupled inductor with the leakage plate, the inductor current ripple is already very small. Increasing switching frequency does not have a significant reduction in ac conduction losses, so the increased switching related losses will dominate. In this case, a higher switching frequency yields a lower efficiency. As for using the coupled inductor without the leakage plate, the inductor current ripple is large. Increasing switching frequency can greatly reduce ac conduction losses. The decreased ac conduction losses dominate the frequency impacts at light load, but at heavy load, the increased switching related losses are predominant. Consequently, a higher switching frequency leads to to a higher efficiency at light load but a lower efficiency at heavy load. At full load where the current ripple amplitude has little influence on the total power losses, the MSC-PoL prototype of using different coupled inductor designs has a similar efficiency for the same switching frequency. The efficiency measurement results indicate that, if excluding the gate losses, the MSC-PoL prototype with the leakage plate can achieve 93.1% peak efficiency at 140 A/400 kHz and 86.2% full-load efficiency at 450 A/400 kHz. In contrast, the MSC-PoL prototype without using the leakage plate can achieve 91% peak efficiency at 150 A/602 kHz and 84.6% at 450 A/602 kHz. The gate drive

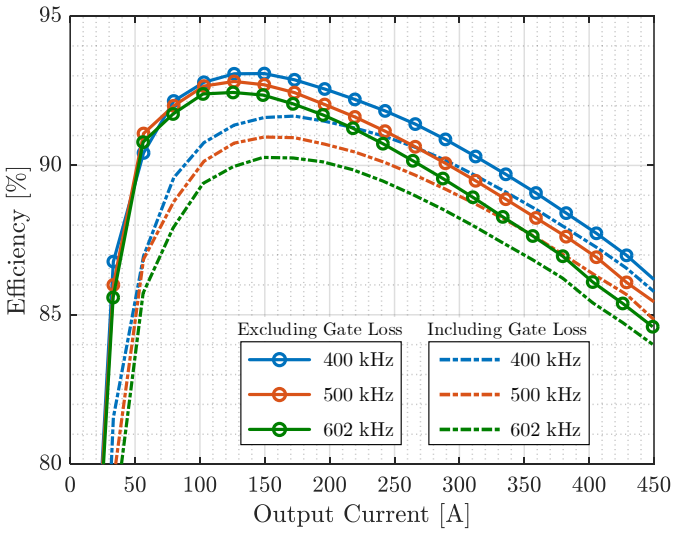

Fig. 32. Measured 48-to-1-V efficiency of the MSC-PoL prototype when using the leakage plate. Efficiencies of different switching frequencies excluding and including the gate losses are plotted and compared. $V_{drive} = 8$ V.

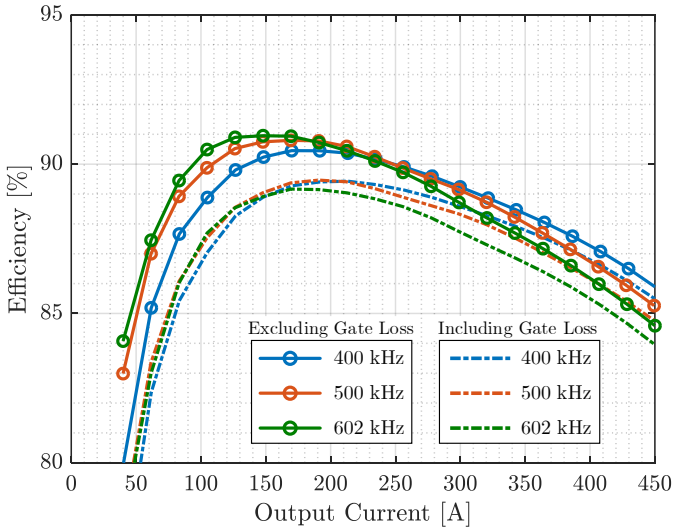

Fig. 33. Measured 48-to-1-V efficiency of the MSC-PoL prototype without using the leakage plate. Efficiencies of different switching frequencies excluding and including the gate losses are plotted and compared. $V_{drive} = 8$ V.

losses are estimated as 2.48 W at 400 kHz, 3.10 W at 500 kHz, and 3.74 W at 602 kHz.

Figure 34 shows the thermal image of the MSC-PoL prototype under DC fan and heat sink cooling. After operating at 450 A full load for more than 10 minutes, the hot-spot temperature of the heat sink maintains around 45 °C when the ambient temperature is around 25 °C. Featuring single-side heat dissipation, the MSC-PoL prototype greatly simplifies its cooling design, enabling long-term operation at heavy load while keeping a cool temperature.

VI. Performance Discussions and Comparison

The 48-to-1-V MSC-PoL CPU VRM is a combination of many state-of-the-art technologies, including multistack SC architecture, soft charging technique, hybrid GaN-Si switch

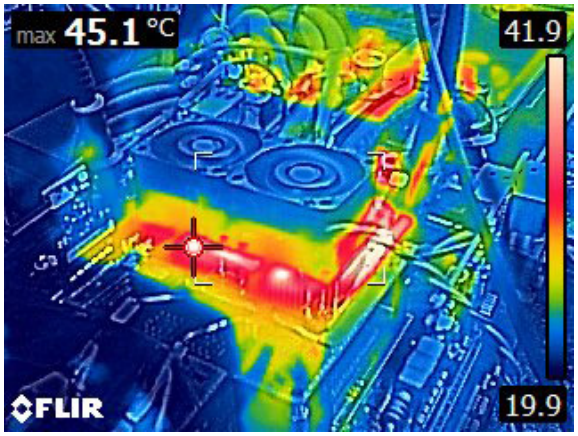

Fig. 34. Thermal image of the MSC-PoL prototype when operating at 48-to-1-V/450-A, $f_{sw} = 400$ kHz under DC fan and heat sink cooling for more than 10 minutes. The hot-spot temperature of the heat sink maintains around 45 °C. The ambient temperature is around 25 °C.

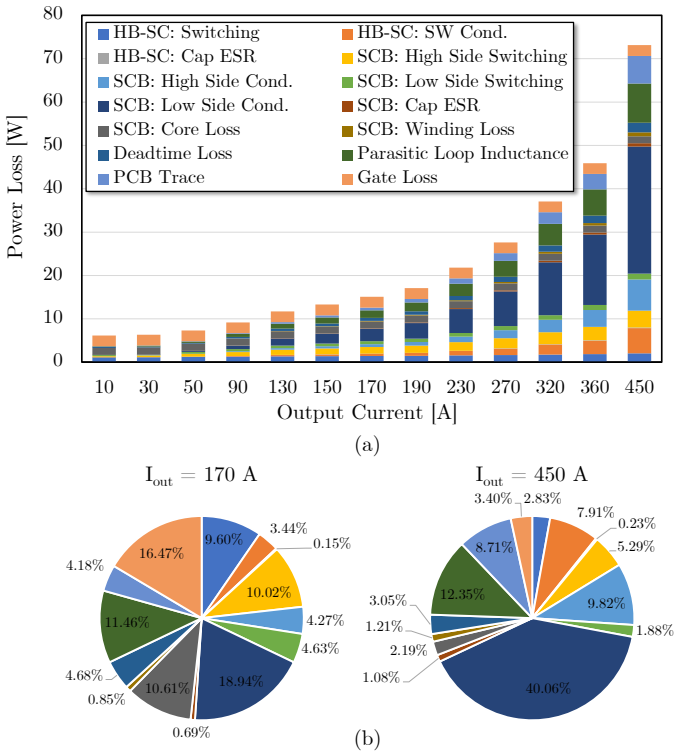

Fig. 35. Loss breakdown of the 48-to-1-V/400 kHz MSC-PoL prototype (with the leakage plate) at (a) full load range and (b) two specific load conditions. Gate loss is included. Power loss listed in the legend is ordered from bottom to top in the bar chart and clockwise from 12 o'clock in the pie charts.

combination, coupled magnetics, and 3D stacked packaging. It achieves an ultra-compact size with both a small area and a low z-height. The overall VRM height is only 6 mm (7 mm if adding the leakage plate), making it an extremely attractive PwrSiP solution for CPU voltage regulation from 48-V.

Appropriate coupled inductor design can be selected based on specific application requirements. Adding the leakage plate can reduce the inductor current ripple, and the resulting smaller RMS and peak current values decrease conduction loss, switching loss, and parasitic inductance loss, yielding

TABLE IV
PERFORMANCE COMPARISON OF THE MSC-POL PROTOTYPE AND OTHER 48 V-TO-1 V POINT-OF-LOAD VOLTAGE REGULATOR DESIGNS

Year	Note	@ Peak Efficiency			@ Full Load			Switching Frequency†	Including Gate Drive Loss & Size
		Output Current	Efficiency	Box Power Density*	Output Current	Efficiency	Box Power Density*		
This Work	Ladder Only 6-mm height	150 A 210 A	91.0% 89.5%	241 W/in^3 338 W/in^3	450 A 450 A	84.6% 85.6%	724 W/in^3 724 W/in^3	602 kHz‡ 400 kHz	Loss ×; Size ✓ Loss ✓; Size ✓
	Ladder + Leakage 7-mm height	140 A 170 A	93.1% 91.7%	193 W/in^3 235 W/in^3	450 A 450 A	86.2% 85.8%	621 W/in^3 621 W/in^3	400 kHz	Loss ×; Size ✓ Loss ✓; Size ✓
2020	Sigma [18]	40 A	94.0%	210 W/in^3	80 A	92.5%	420 W/in^3	600 kHz	Loss ×; Size ✓
2020	TSAB [43]	30 A	91.5%	12 W/in^3	90 A	85.0%	36 W/in^3	500 kHz	Loss ×; Size ✓
2020	Vicor [44], [45]	120 A	90.1%	224 W/in^3	214 A	87%¶	400 W/in^3	1,025 kHz	Loss ✓; Size ✓
2021	ADI [46]	30 A	90.8%	53.1 W/in^3	50 A	88.1%	88.5 W/in^3	350 kHz	Loss ✓; Size ✓
2021	On-Chip [30]	1.5 A	90.2%	37.1 W/in^3	8 A	76%	198 W/in^3	2,500 kHz	Loss ✓; Size ✓
2021	LEGO-PoL [25]	190 A	88.4%	124 W/in^3	450 A	84.8%	294 W/in^3	1,000 kHz	Loss ✓; Size ✓
2021	VIB-PoL [13]	144 A	93.3%	74.2 W/in^3	450 A	88.1%	232 W/in^3	417 kHz	Loss ✓; Size ✓
2022	MLB-PoL [47]	23 A	91.5%	101 W/in^3	60 A	88.4%	263 W/in^3	250 kHz	Loss ✓; Size ✓
2022	Symmetric-DIH [48]	36 A	81.4%§	205 W/in^3	105 A	70.9%§	598 W/in^3	750 kHz	Loss ✓; Size ✓
2022	Dickson^2-PoL [36]	100 A	91.6%	133 W/in^3	270 A	87.7%	360 W/in^3	280 kHz	Loss ✓; Size ✓
2023	Mini-LEGO [49]	160 A	84.1%	929 W/in^3	240 A	82.3%	1,390 W/in^3	1,515 kHz	Loss ✓; Size ✓

∗ The power density is calculated with the box volume (defined as the maximum Length×Width×Height) of the prototype.
† The switching frequency of the voltage regulation stage.
‡ The frequency of the MSC-PoL prototype is selected for the maximum peak efficiency with or without the gate drive loss.
¶ The full load efficiency of the Vicor product is not available and is estimated.
§ Efficiency including gate loss for Symmetric-DIH is calculated based on the gate driving energy per switching cycle provided in [48].

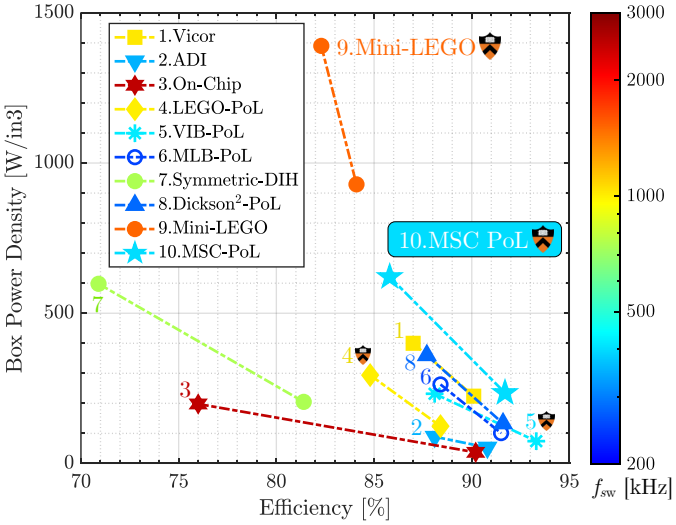

Fig. 36. Performance comparison of the MSC-PoL prototype (with the leakage plate) and other 48-to-1-V VRMs. Efficiency and power density points (including gate loss and size) at full load and peak-efficiency load are plotted and connected with a line. Switching frequencies are color coded, corresponding to the logarithmic color bar. The MSC-PoL VRM achieves both excellent efficiency and power density among state-of-the art VRM designs.

a higher efficiency. The tradeoff is the increased VRM height and slower transient response. However, with 8-phase (or 16-phase) interleaving, the coupled inductor that uses the leakage plate can still achieve a fast transient speed, as demonstrated in Section V-C. Although the light-load efficiencies for the two coupled inductor designs are quite different, their heavy-load efficiencies are very close given the same operation frequency.

Detailed loss breakdown of the 48-to-1-V/400 kHz MSC-PoL prototype (with the leakage plate) is plotted in Fig. 35. The power loss breakdown contains 1) losses of the H-Bridge SC stage including switching and conduction losses of the GaN switches ($S_{0X} \sim S_{1X}$) as well as ESR loss of the flying capacitors (C_{fly}); 2) losses of the SCB stage including switching and conduction losses of the MOSFETs ($S_{2X} \sim S_{8X}$), ESR loss of the blocking capacitors ($C_{1X} \sim C_{3X}$), core loss and winding loss of the coupled inductors; 3) parasitic loop inductance loss estimated by $\frac{1}{2}L_{loop}i_L^2 f_{sw}$; 4) deadtime loss, PCB trace conduction loss, and gate loss estimated by $Q_g V_{drive} f_{sw}$. At light load, gate loss, core loss, and switching loss are predominant. When load current increases to 170 A where the peak efficiency is achieved, the major power losses are relatively evenly distributed among switching loss, conduction loss, and gate loss. As load current keep rising, the low-side conduction loss and parasitic loop inductance loss increase dramatically and will dominate at 450 A full load. To further improve the efficiency and power density, multiple switches and gate drivers can be integrated together to reduce the parasitic loop inductance especially for the SCB stage.

Table IV compares several key metrics of the MSC-PoL prototype with other state-of-the-art 48 V-to-1 V point-of-load voltage regulators. The full-load power density with and without using the leakage plate is 621 W/in^3 and 724 W/in^3, respectively. A performance metric represented as the connection curve of the efficiency and power density points at

full load and peak-efficiency load is introduced and plotted in Fig. 36. The MSC-PoL prototype presented in this paper expands the performance boundary of point-of-load VRMs by pushing towards higher efficiency and higher power density.

VII. Conclusions

This paper presents the MSC-PoL PwrSiP VRM with coupled magnetics to power ultrahigh-current CPU or chiplet systems. In the MSC-PoL architecture, many SC cells are stacked in front and connected with switched inductor cells for soft charging and voltage regulation. It attains decreased current ripple and boosted transient speed from parallel coupling as well as reduced charge sharing loss and automatic capacitor-voltage/inductor-current balancing from soft charging. A 48-to-1-V MSC-PoL topology is developed and its steady-state and transient performance are analyzed. The 48-to-1-V MSC-PoL converter has a similar small signal model and transfer functions as a multiphase buck. Therefore, typical buck control methods (e.g., voltage-mode and constant-on-time controls) can be directly applied with a 25% duty ratio limit. To validate the MSC-PoL architecture, a 48-to-1-V/450-A prototype containing two MSC-PoL modules is built. Two coupled inductor designs based on a ladder-structured magnetic core are developed and compared. A leakage magnetic plate of 0.8-mm thickness is designed to adjust the leakage inductance for lower current ripple. Benefiting from the 3D stacked inductor-driver packaging, one MSC-PoL module encloses all circuits and components into a $\frac{1}{16}$-brick/0.31-in^3/6-mm-thick package, achieving 724 W/in^3 power density. It leverages a hybrid GaN-Si switch combination for maximized benefits from the latest GaN and Silicon devices. When including the gate loss, the MSC-PoL prototype with the leakage plate can achieve 91.7% peak efficiency at 170 A/400 kHz and 85.8% full-load efficiency at 450 A/400 kHz. In contrast, the MSC-PoL prototype without using the leakage plate can achieve 89.5% peak efficiency at 210 A/400 kHz and 85.6% at 450 A/400 kHz. The MSC-PoL VRM achieves both excellent efficiency and power density compared to state-of-the art VRM designs. It can be further embedded into the CPU/chiplet socket for PwrSiP voltage regulation with extreme efficiency, density, and control bandwidth.

Appendix I
Derivations of the Small-Signal Model

This appendix presents the detailed derivations for the small signal model. According to Fig. 11, dynamic modeling equation for each phase can be obtained as:

$$\begin{cases} D\left(\hat{v}_{Cfly}-\hat{v}_{C1A}\right)+\left(V_{Cfly}-V_{C1A}\right)\hat{d}=f(\hat{i}_{L1A}) \\ D\left(\hat{v}_{C1A}-\hat{v}_{C2A}\right)+\left(V_{C1A}-V_{C2A}\right)\hat{d}=f(\hat{i}_{L2A}) \\ D\left(\hat{v}_{C2A}-\hat{v}_{C3A}\right)+\left(V_{C2A}-V_{C3A}\right)\hat{d}=f(\hat{i}_{L3A}) \\ D\cdot\hat{v}_{C3A}+V_{C3A}\cdot\hat{d}=f(\hat{i}_{L4A}), \end{cases}$$
$$\begin{cases} D\left(\hat{v}_{in}-\hat{v}_{Cfly}-\hat{v}_{C1B}\right)+\left(V_{in}-V_{Cfly}-V_{C1B}\right)\hat{d}=f(\hat{i}_{L1B}) \\ D\left(\hat{v}_{C1B}-\hat{v}_{C2B}\right)+\left(V_{C1B}-V_{C2B}\right)\hat{d}=f(\hat{i}_{L2B}) \\ D\left(\hat{v}_{C2B}-\hat{v}_{C3B}\right)+\left(V_{C2B}-V_{C3B}\right)\hat{d}=f(\hat{i}_{L3B}) \\ D\cdot\hat{v}_{C3B}+V_{C3B}\cdot\hat{d}=f(\hat{i}_{L4B}). \end{cases} \tag{8}$$

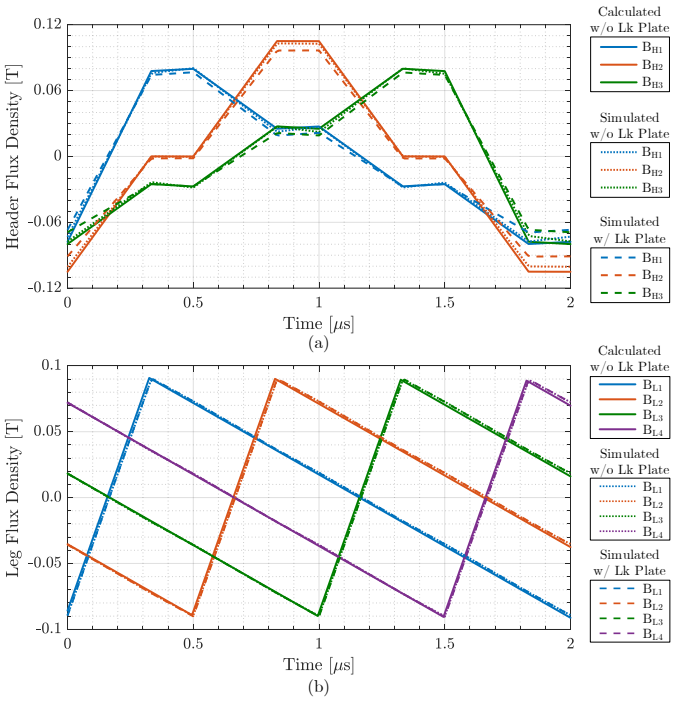

Fig. 37. Calculated and ANSYS-simulated magnetic flux density in: (a) each core header ($B_{H1} \sim B_{H3}$) and (b) each core leg ($B_{L1} \sim B_{L4}$). $V_o = 1$ V; $D = \frac{1}{6}$; $f_{sw} = 500$ kHz.

Here, $f(\hat{i}_{LkX})$ ($k = 1 \sim 4$, $X = A$ or B) is the voltage drop across the inductor winding, the R_{eq}, and the output port at each phase:

$$f(\hat{i}_{LkX}) = s\sum_{n=1}^{4} L_{kn}\hat{i}_{LnX} + \hat{i}_{LkX}R_{eq} + \hat{v}_o. \tag{9}$$

By summing up the equations in (8), impacts of the flying capacitor (C_{fly}) and the blocking capacitors ($C_{1X} \sim C_{3X}$) are eliminated, and the overall converter dynamic equation can be derived as shown in Eq. (3).

Appendix II
Derivations of the Magnetic Flux Density

This appendix analytically derives the ac magnetic flux density in a ladder-structured coupled inductor based on its inductance dual model. The presented MSC-PoL converter operates the four-phase coupled inductor similarly to an interleaved multiphase buck: four windings are driven by interleaved square wave voltages shifting between $(1-\frac{1}{D})v_o$ and v_o. Denote the winding voltages as $v_{L1} \sim v_{L4}$, which can be expressed as:

$$v_{Lk} = \begin{cases} \left(1-\dfrac{1}{D}\right)v_o & \dfrac{(k-1)T}{4} \le t < (D+\dfrac{k-1}{4})T \\ v_o & \text{Otherwise} \end{cases}. \tag{10}$$

The magnetic flux of each segment in the ladder magnetic core can be mapped to the corresponding inductor current in the inductance dual model. As shown in Fig. 14b, the ac current of the inductor $1/\mathcal{R}_L$ is directly determined by its

parallel voltage source: $\mathrm{d}i_{\mathcal{R}_{Lk}}/\mathrm{d}t = v_{Lk} \cdot \mathcal{R}_L$. Accordingly, the ac flux density in the k$^{\text{th}}$ core leg can be derived:

$$B_{Lk} = \frac{1}{S_{Leg}} \cdot \frac{i_{\mathcal{R}_{Lk}}}{\mathcal{R}_L} = \frac{1}{S_{Leg}} \int v_{Lk} \mathrm{d}t. \tag{11}$$

S_{Leg} is the cross-sectional area of each core leg. Eq. (11) can also be developed from Faraday's law. It implies that the ac flux density in one core leg is only related to its own winding voltage, irrelevant to other phases.

In Fig. 14b, $1/\mathcal{R}_H >> 1/\mathcal{R}_K$ even with the leakage plate. Therefore, the voltage across the inductor $1/\mathcal{R}_H$ is primarily determined by the voltage division along the series-connected $1/\mathcal{R}_{K1} \sim 1/\mathcal{R}_{K4}$. Similar to Eq. (11), the ac flux density in core headers (i.e., segments between core legs) can be derived:

$$\begin{cases} B_{H1} = \dfrac{1}{S_{Head}} \displaystyle\int \left(v_{L1} - \sum_{j=1}^{4} v_{Lj} \cdot \frac{\frac{1}{\mathcal{R}_{K1}}}{\sum_{j=1}^{4} \frac{1}{\mathcal{R}_{Kj}}} \right) \mathrm{d}t, \\ B_{H2} = \dfrac{1}{S_{Head}} \displaystyle\int \left(v_{L1} + v_{L2} - \sum_{j=1}^{4} v_{Lj} \cdot \frac{\frac{1}{\mathcal{R}_{K1}} + \frac{1}{\mathcal{R}_{K2}}}{\sum_{j=1}^{4} \frac{1}{\mathcal{R}_{Kj}}} \right) \mathrm{d}t, \\ B_{H3} = \dfrac{1}{S_{Head}} \displaystyle\int \left(-v_{L4} + \sum_{j=1}^{4} v_{Lj} \cdot \frac{\frac{1}{\mathcal{R}_{K4}}}{\sum_{j=1}^{4} \frac{1}{\mathcal{R}_{Kj}}} \right) \mathrm{d}t. \end{cases} \tag{12}$$

S_{Head} is the cross-sectional area of each core header; $\mathcal{R}_{K1} \sim \mathcal{R}_{K4}$ can be obtained from the extracted inductance matrix in ANSYS simulation. In Section IV-A, to simplify the calculation, $\mathcal{R}_{K1} \sim \mathcal{R}_{K4}$ are treated as identical in the inductor optimization process, as their differences are small.

Figure 37 compares the calculated and simulated ac flux density for the two coupled inductor designs. As indicated in the figure, the ac flux density is almost the same with or without using the leakage plate. The calculated and simulated results match well, validating the theoretical analysis.

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